

YAMAHA

COMBO SYNTHESIZER

CS-30



SERVICE MANUAL

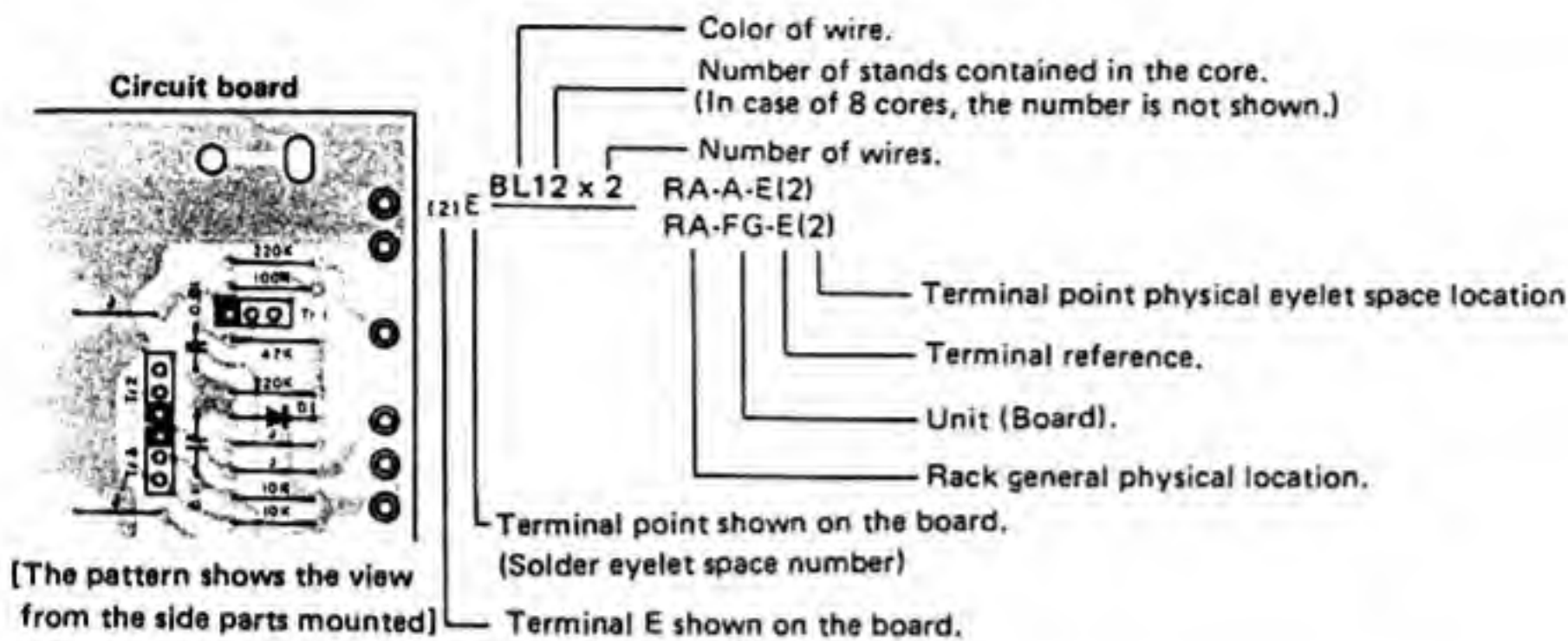
INDEX (目 次)

CORDING GUIDE(活用の手引)	1
DISASSEMBLY PROCEDURE(分解手順)	2
SPECIFICATIONS(総合仕様)	3
PANEL LAYOUT(パネル レイアウト)	4
SSK Circuit Diagram (SSKシート図).....	5
SSK Circuit Board & Wiring (SSKシート基板図)	6
VCO Circuit Diagram (VCOシート図).....	7
VCO Circuit Board & Wiring (VCOシート基板図)	8
VCF Circuit Diagram (VCFシート図).....	9
VCF Circuit Board & Wiring (VCFシート基板図).....	10
VCA Circuit Diagram (VCAシート図)	11
VCA Circuit Board & Wiring (VCAシート基板図)	12
SEQ Circuit Diagram (SEQシート図)	13
SEQ Circuit Board & Wiring (SEQシート基板図)	14
LFO Circuit Diagram (LFOシート図)	15
LFO Circuit Board & Wiring (LFOシート基板図)	16
PRA Circuit Diagram (PRAシート図)	17
PRA Circuit Board & Wiring (PRAシート基板図)	18
ADC Circuit Diagram (ADCシート図)	19
ADC Circuit Board & Wiring (ADCシート基板図)	19
KEY SWITCH Circuit Diagram (鍵盤シート図).....	20
PN3 Circuit Diagram (PN3シート図).....	20
REAR PANEL Circuit Diagram (リアーパネルシート図)	21
REAR PANEL Circuit Board & Wiring (リアーパネルシート基板図).....	21
Standard for circuit inspection and adjustment (シート検査調整基準).....	22~37
PARTS LIST (パーツリスト)	

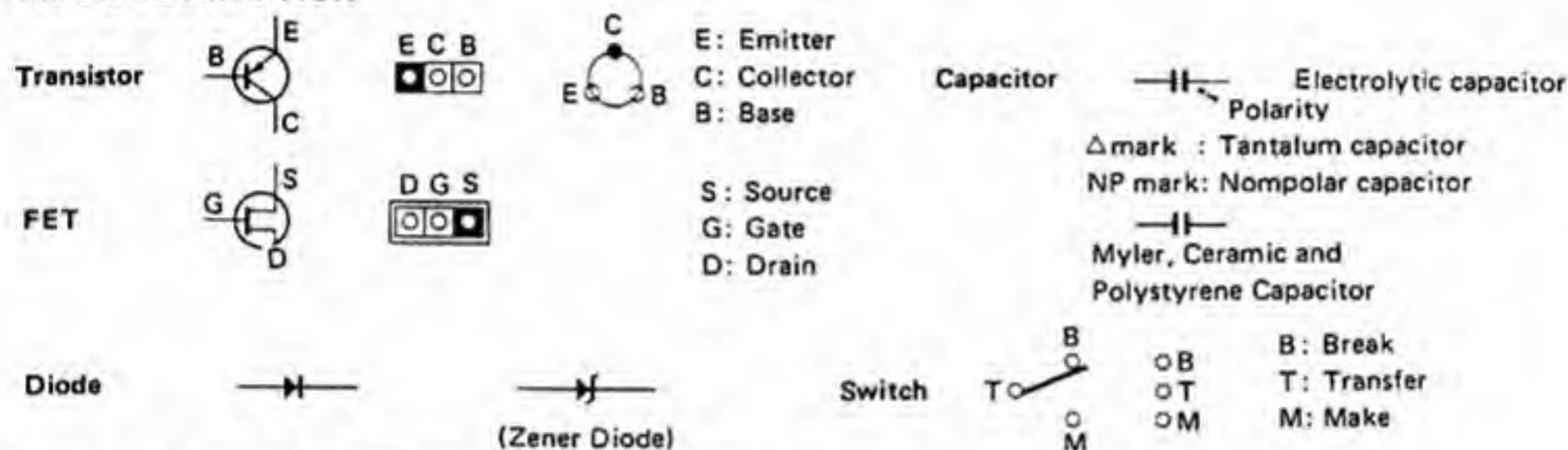
CORDING GUIDE (活用の手引)

1 CIRCUIT BOARD AND WIRING

Two (2) black wires are connected to "E" on circuit board. One goes to each "E" terminal of A and FG circuit boards. In this case, the coding system is as follows:



2 SYMBOL DESCRIPTION



3 ABBREVIATIONS OF WIRE COLOR IN ELECTONE

BLACK	BL	BROWN	BR	RED	RE
ORANGE	OR	YELLOW	YE	GREEN	GR
BLUE	BE	VIOLET	VI	GRAY	GY
WHITE	WH	GRASS GREEN	GG	SKY BLUE	SB
PINK	PK	TRANSPARENT	TR		

4 WIRE COLOR - Musical Note Indication

C	C#	D	D#	E	F	F#	G	G#	A	A#	B
BR	RE	OR	YE	GR	BE	VI	GY	WH	GG	SB	PK

5 LOGIC SYMBOL

	MIL R	YAMAHA
NOT		
NOR		
NAND		

Exclusive OR

Truth Table

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

NOT (Inverter)

Truth Table

A	Y
0	1
1	0

Truth Table

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

Truth Table

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

Truth Table

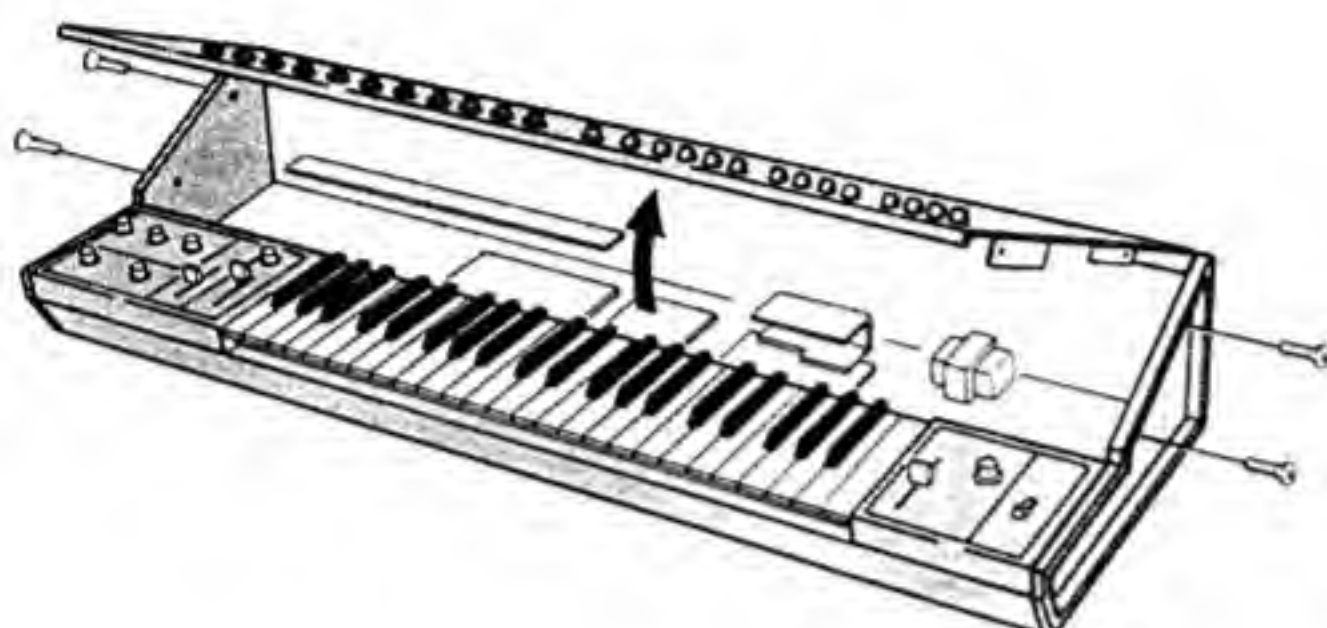
A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

Truth Table

A	B	Y
0	0	1
1	0	1
0	1	1
0	0	0

DISASSEMBLY PROCEDURE (分解手順)

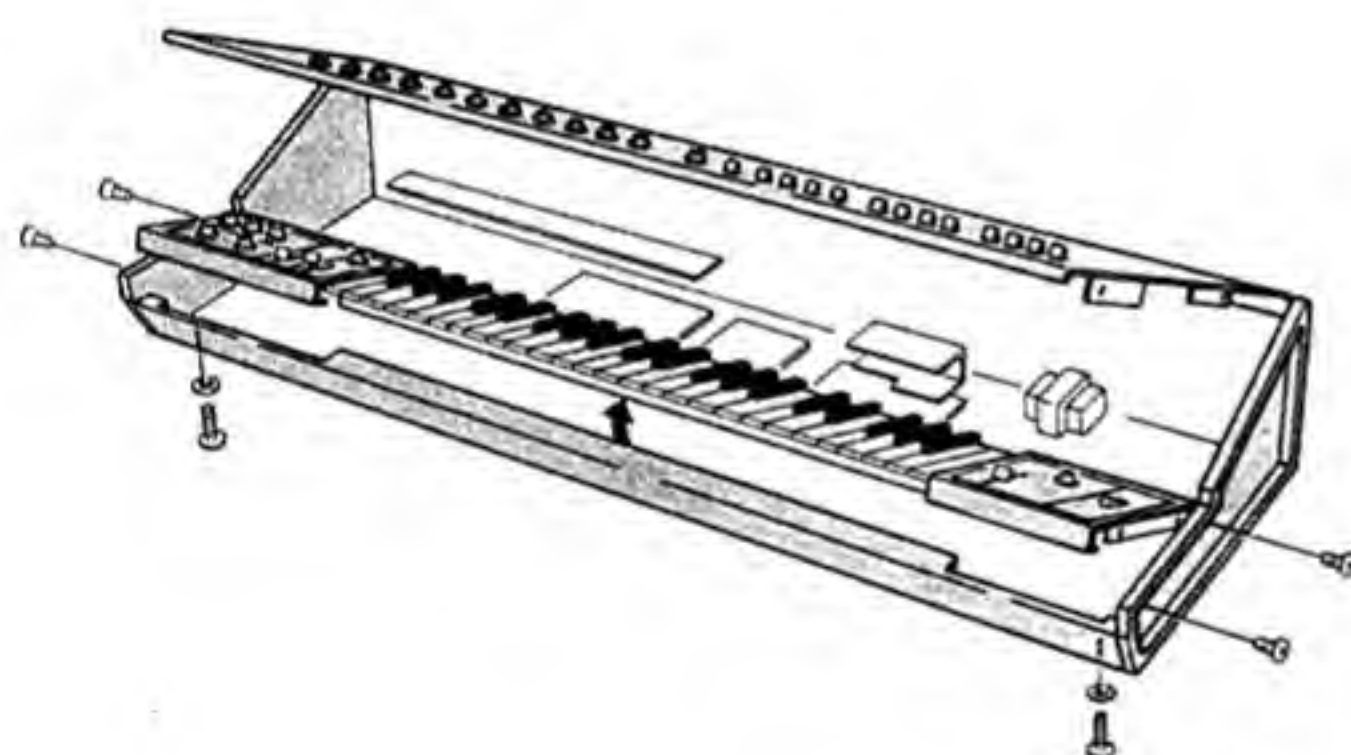
Removal of Panel パネルの取り外し



Remove all screws illustrated above and take away the panel, lifting it up gently.

図の各ネジを外し、パネルを上へ持ち上げながら取り外して下さい。

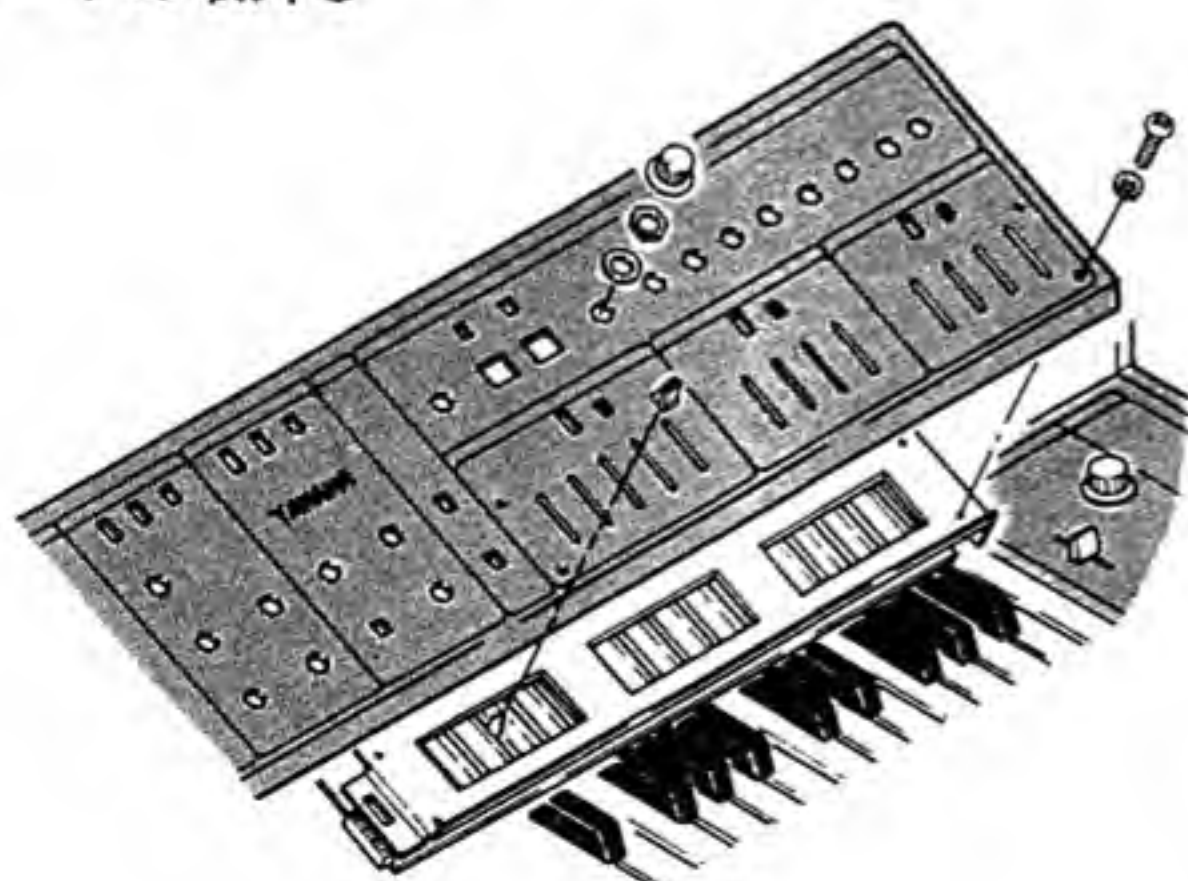
Removal of Keyboard 鍵盤の取り外し



After removing the panel, pulling out the screws as shown above permits rotating the keyboard.

パネルを取り外した後、図の各ネジを外しますと鍵盤を回転させる事ができます。

Removal of Circuit Boards シートの取外し



Take the circuit boards away gently from the panel, removing each volume knob and hexagonal nut without any damage or scratch on the panel.

パネルを傷付けない様に各ボリュームのつまみと六角ナットを外して、シートをパネルから静かに外して下さい。

SPECIFICATIONS (総合仕様)

Keyboard 44 keys, 3½ octaves

CONTROLS

PITCH TUNE: +65 cents to -65 cents
DE TUNE; VCO 1: +700 cents
to -500 cents

EG: SELECTOR, DEPTH

VCO KEY VOLT: SEQ/KBD
FEET;
VCO 1: 2' 4' 8' 16' 32' 64'
VCO 2: 4' 8' 16' 32' 64' 128'
PW: 50~90%

PWM: 10 ~ 90% (LFO sine)

MOD VCO 2 (VCO 1)

MODULATION: FUNCTION,
DEPTHVCF VCF1 INPUT: \backslash / Π VCO1/ \backslash
VCO LEVEL
VCO2/NOISE/
EXT LEVEL
VCF2 INPUT: VCF1H/ \backslash / Π
VCO2

KBD FOLLOW

MODULATION: FUNCTION,
DEPTH

CUT OFF FRQ

RESONANCE

EG: SELECTOR, DEPTH

VCA FILTER: HP/BP/LP

VCA 1; Input selectors: VCF
1, VCF 2 and \sqrt VCO 1RMO(VCA2): NORMAL/RMO
VCO1/LFO

HOLD: HOLD/EG

EG selector: A, C and E

MODULATION: FUNCTION,
DEPTHTRIGGER LFO/NORMAL,
SINGLE/MULTISEQUENCER CLOCK SPEED: 0.1~30Hz
STEP: 1 to 8
NORMAL/KBD
CLOCK/MANUAL
MANUAL/START or STOP
HOLD
PITCH: 1 to 8EG TRIGGER: KBD/SEQ/EXT
EG TIME: NORMAL/TIMEx5

EG 1; IL . . . 0 ~ -5

AL . . . 0 ~ +5

AT . . . 1msec.~ 1sec.

DT . . . 10msec.~10sec.

RT . . . 10msec.~10sec.

EG2, 3; AT . . . 1msec.~1sec.

DT . . . 10msec.~10sec.

SL . . . 0 ~ 10

RT . . . 10msec.~10sec.

LFO EG: FUNCTION, DEPTH
SPEED: 0.1 ~ 100Hz

EXTERNAL Sensitivity: 0/-20 (dBm)

TRIGGER LEVEL: Trigger
ON at 60mV_{p-p} (Min.)

SIGNAL LEVEL

PORTAMENTO 4sec. at LONG

PITCH BEND ±1 octave at LIMITTER max.

OUTPUT BALANCE, VOLUME

TERMINALS

OUTPUT 1, 1+2, 2;

HIGH: 0dBm/600Ω

LOW: -20dBm/600Ω

FOOT CONTROLLER for volume control

SEQUENCER OUT . . CONTROL VOLT, TRIGGER

KEY VOLT IN/OUT

TRIGGER IN/OUT

EXTERNAL IN

PHONES for headphones

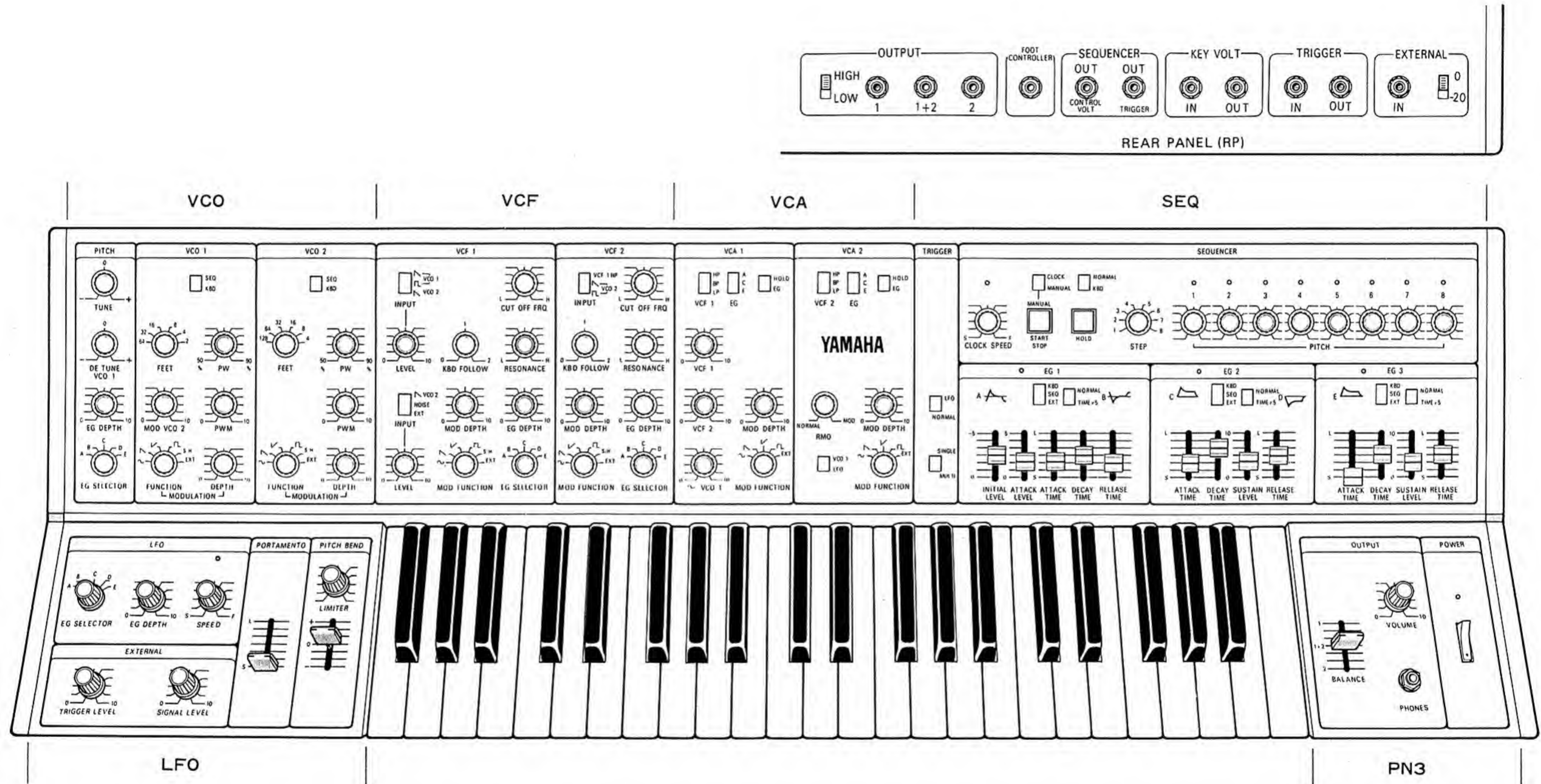
POWER SOURCE: AC 50/60 Hz

POWER CONSUMPTION: 40W

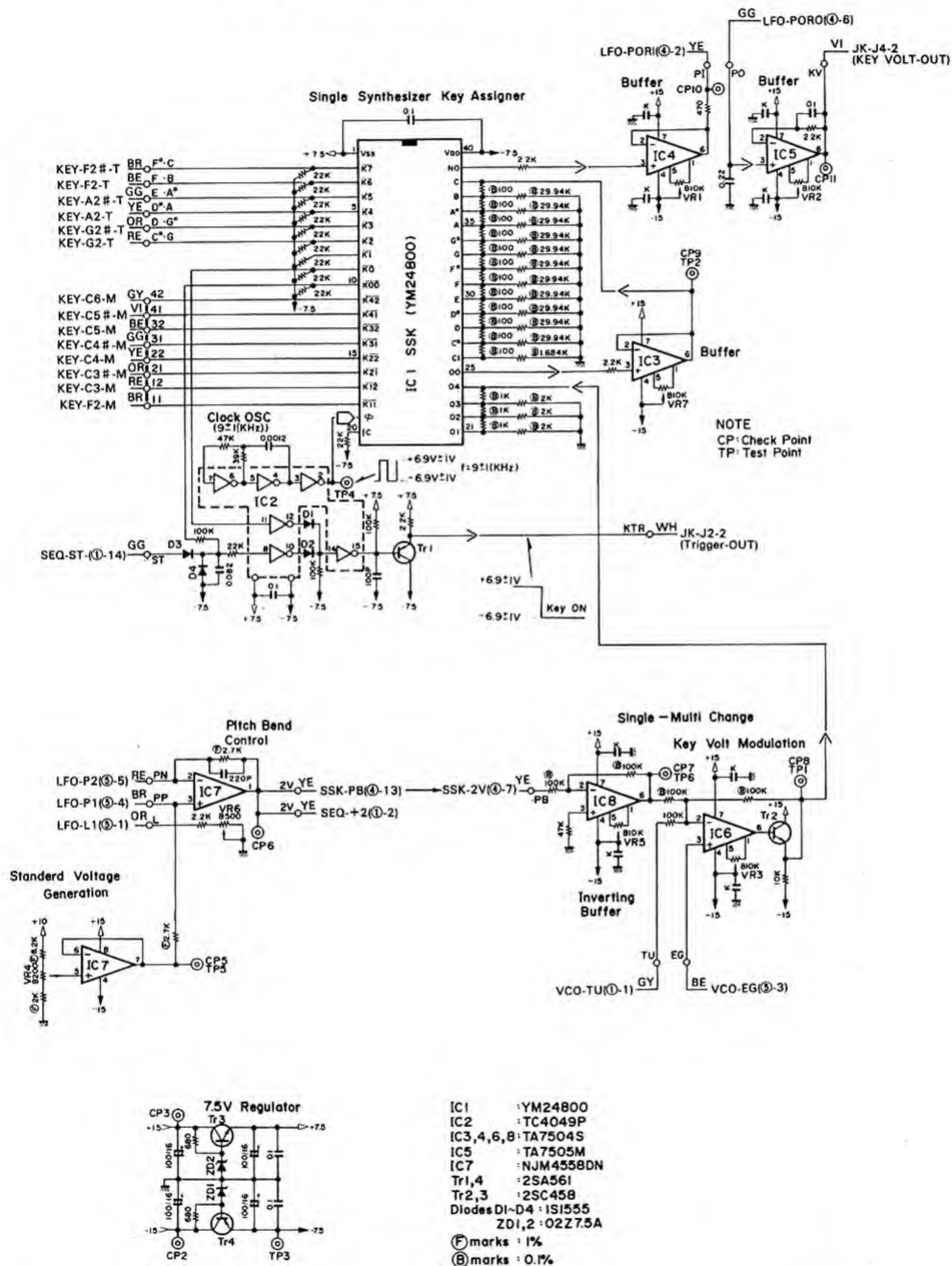
DIMENSIONS 978(W) x 330(D) x 173(H) mm
38½(W) x 13(D) x 6-13/16(H) in.

WEIGHT 15kg, 33.0 lbs

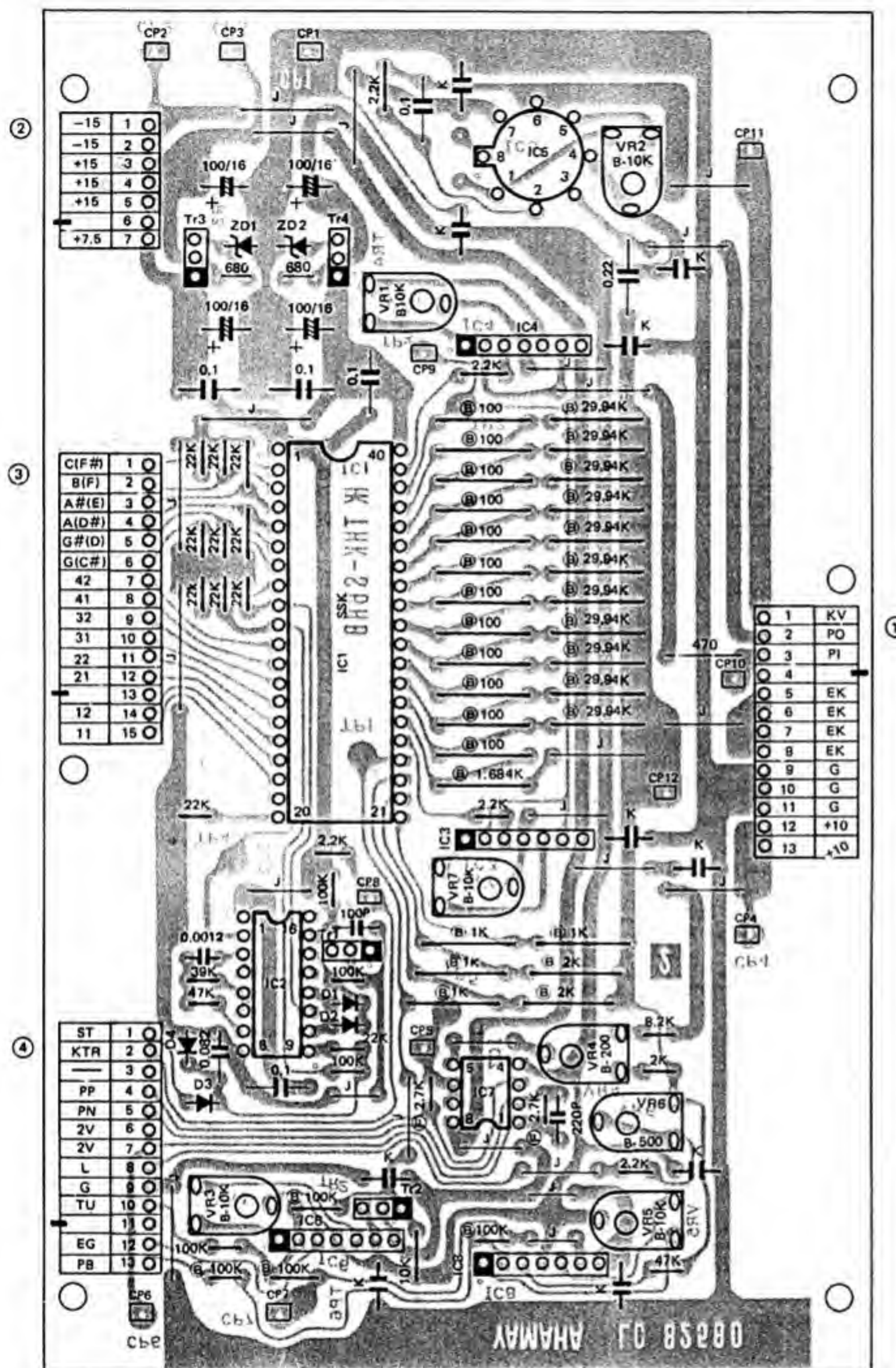
PANEL LAYOUT (パネルレイアウト)



SSK Circuit Diagram



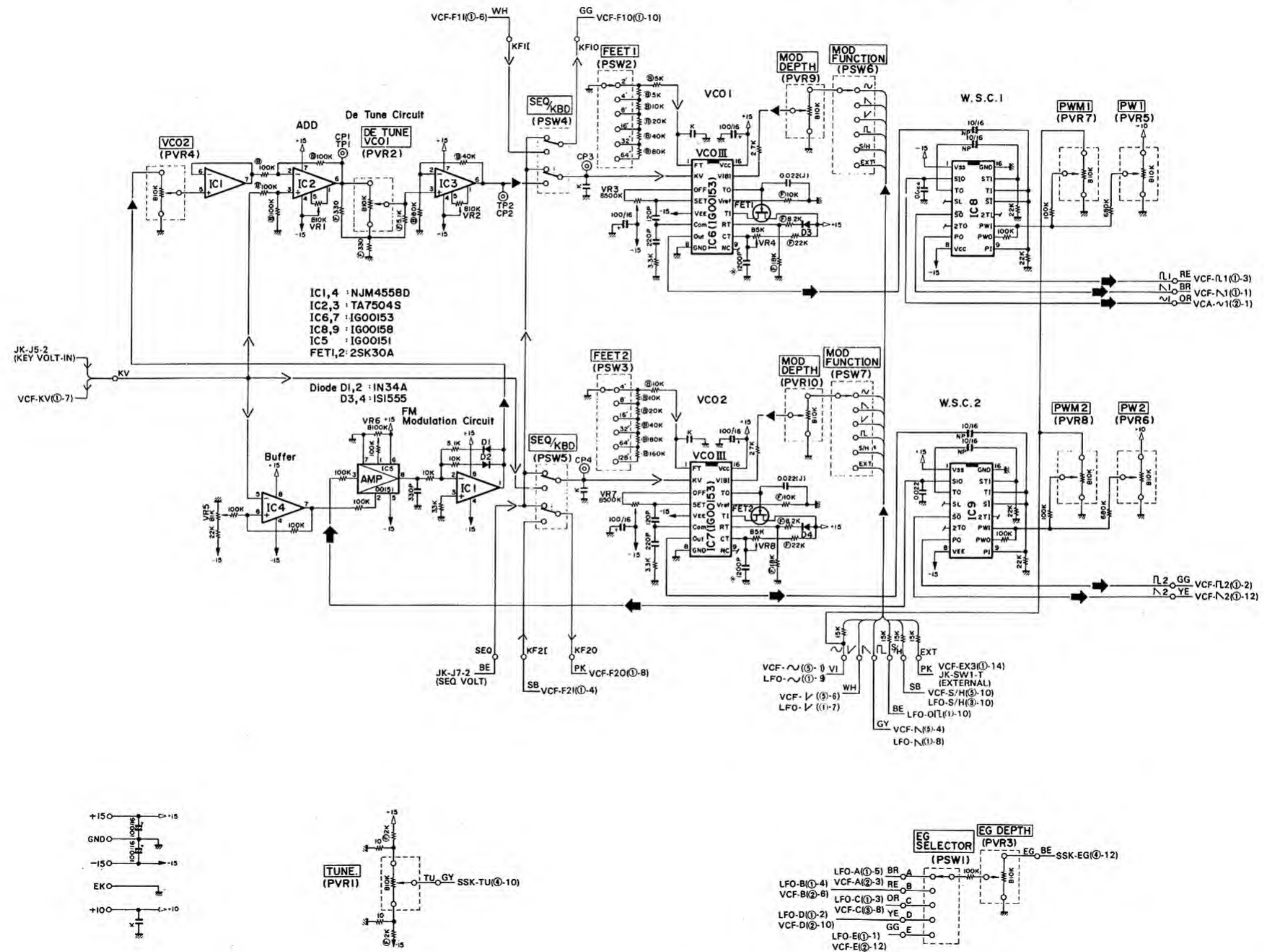
SSK Circuit Board & Wiring



(Note)

- IC
 - IC1 : YM24800
 - IC2 : TC4049
 - IC3,4,6,8 : TA7504
 - IC5 : TC7505
 - IC7 : NJM4558
- Transistor (トランジスタ)
 - Tr1,4 : 2SA561
 - Tr2,3 : 2SC458
- Resistor (抵抗)
 - ⓕ marks : $\pm 1\%$
 - ⓑ marks : $\pm 0.1\%$
- Diode (ダイオード)
 - ZD1,2 : 02Z7.5A
 - D1 ~ 4 : 1S1555
- Semi variable resistor (半固定抵抗)
 - V8K4-1 Type

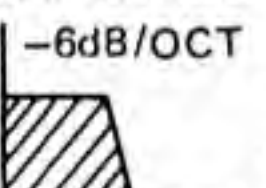
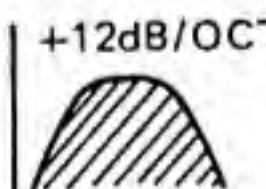

KFC-90107-78A

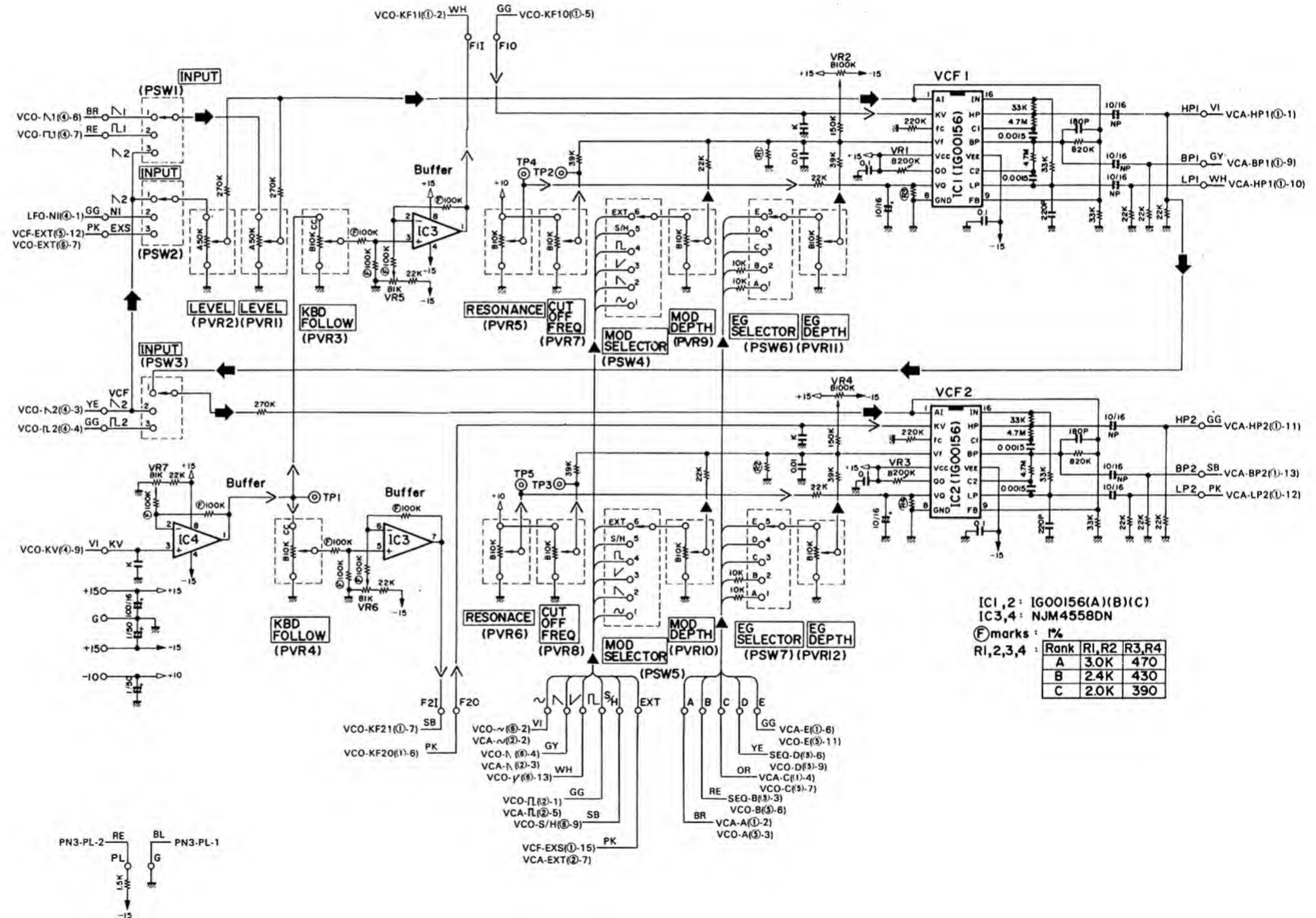


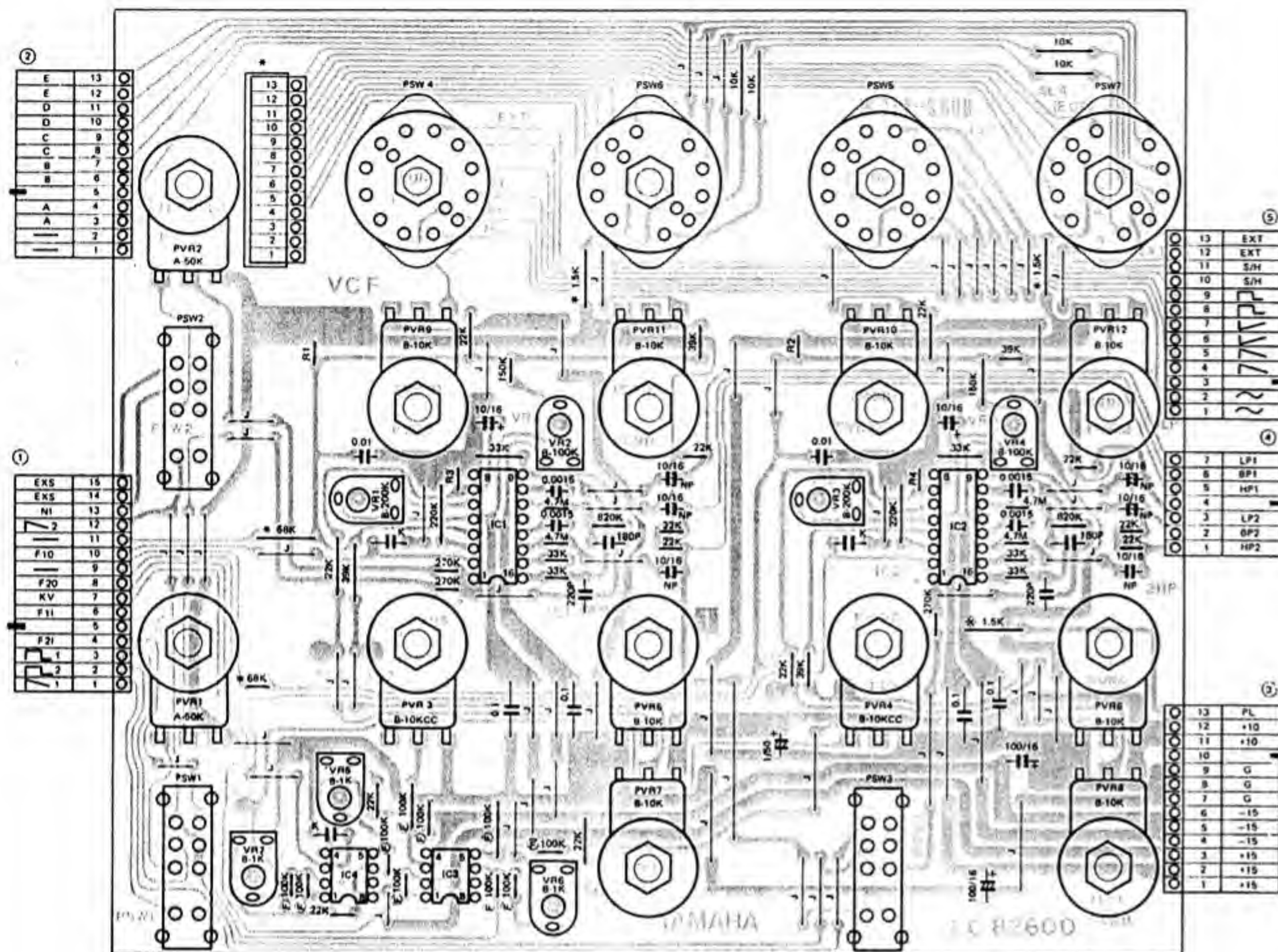
--- Explanation for IC
(IC説明)

VCF Circuit Diagram

VCF IC (IG00156)

1. AI Signal Input
Input signals from VCO are provided to this pin.
2. KV Key voltage input
In order to change the tone color according to the tone range of keyboard, the designated voltage of the key will be supplied to the pin. (0.25-4.0V)
3. f_c Adjustment of the cut off frequency.
Set the control current of the cut off frequency.
4. V_f Input of the cut off voltage.
Input voltage of cut off frequency is supplied to this pin so that the tone color can be changed. The center point of the cut off frequency can be also set.
When the VK is 0.25V and V_f is 5V, the cut off frequency is set to just 1KHz.
5. V_{cc} +15V input power source
6. Q0 Q adjustment.
The Q control current sets the Q equal to 10, when VQ is 0 volt.
7. VQ Input of the voltage for Q control.
Q is variable according to the control voltage supplied.
When the control voltage is 0V (Max.), Q=10
When the control voltage is 10V (Min.), Q=0.5
8. GND Earth
9. FB Q feed back
This is the feed back output pin for the Q control by which the Q is determined.
10. LP Low-pass output
 The output of lower frequencies are produced.
11. C2 C pin for determination of the cut off frequency.
12. Vee -15V power source.
13. BP Band-pass output.
 The output of intermediate frequencies are produced.
14. C1 C pin for determination of the cut off frequency.
15. HP Hi-pass output
 The output of higher frequencies are produced.
16. IN Input of feed back
The input signal for determination of cut off frequency.





* mark : CS-30L only
* mark : CS-30 only

View from the printed pattern side of the circuit board.
パターン側から見た部品配置です。

(Note)

1. IC
IC1,2 : IG00156
IC3,4 : NJM4558
2. Resistor
ⓕ marks : $\pm 1\%$
R1R2R3R4: Rank of IC1,2

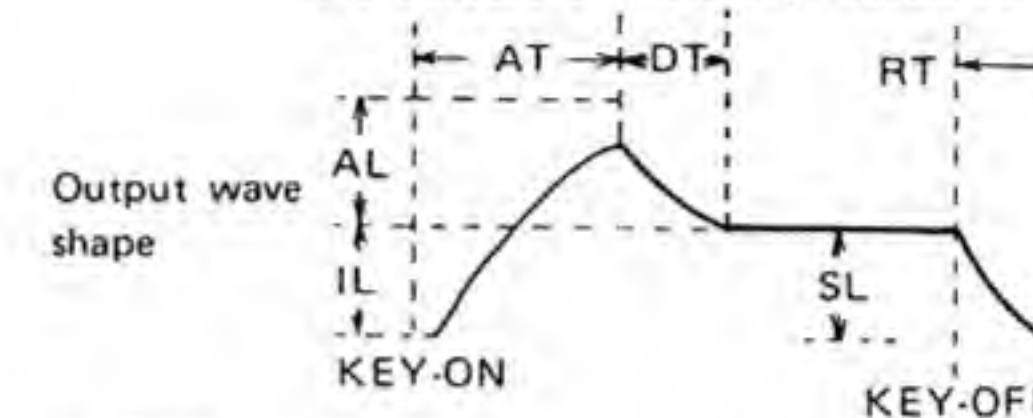
IC Rank	R1R2	R3R4
A	3K	470
B	2.4K	430
C	2K	390

VCF-EG (IG00152)

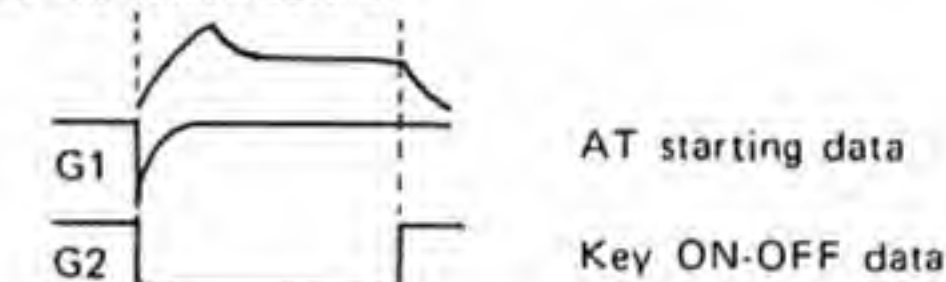
This IC generates envelope wave shape which is supplied to VCF and control the tone color.

1. NC Not connected
2. BI Input of buffer amplifier.
3. OUT Output of buffer amplifier.

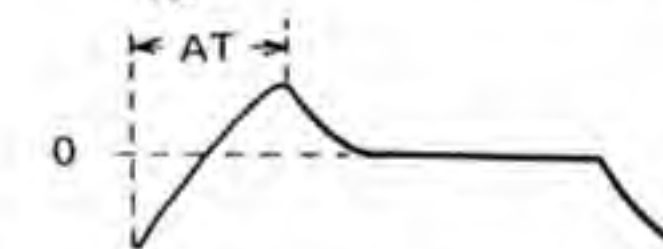
The buffer amplifier is built in for the purpose of matching impedance.



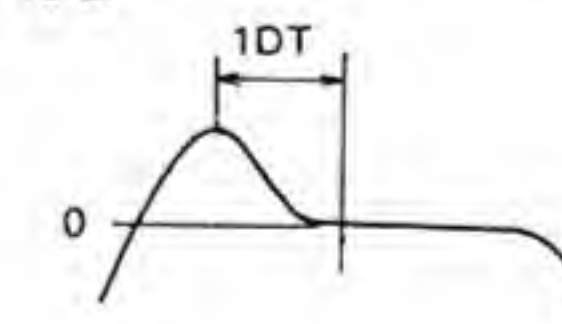
4. GND Earth
5. Vcc +15V input power source.
6. G1 Gate 1
7. G2 Gate 2



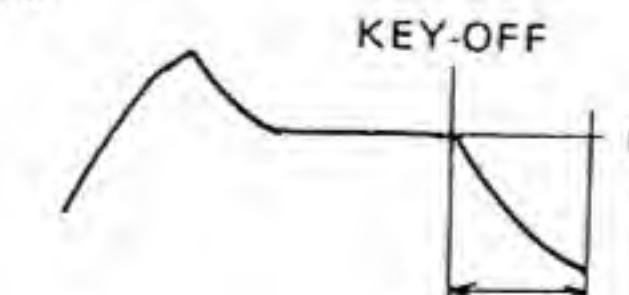
8. Vee -15V input power source.
9. AT Input of buffer voltage for determination of the attack time.
Input of the voltage between zero V and 10V is provided and the attack time is controlled from 1 mS until 1S.



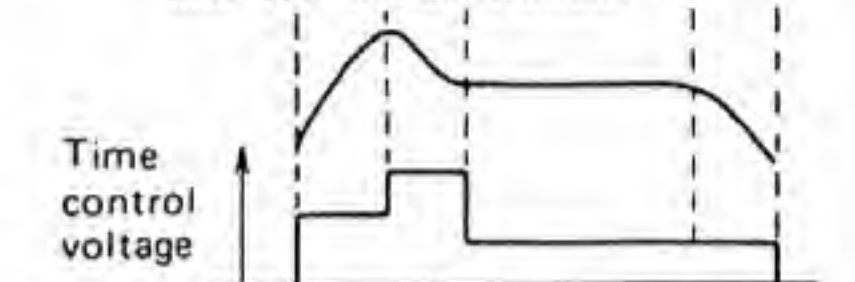
10. DT Input of buffer voltage for determination of the decay time.
Input of the voltage between zero V and 10V is provided and the first decay time is controlled from 10mS until 10 S.



11. RT Input of buffer voltage for determination of the release time.
Input of the voltage between zero V to 10V is provided and the time from KEY-ON until release is controlled from 10m second until 10 second.

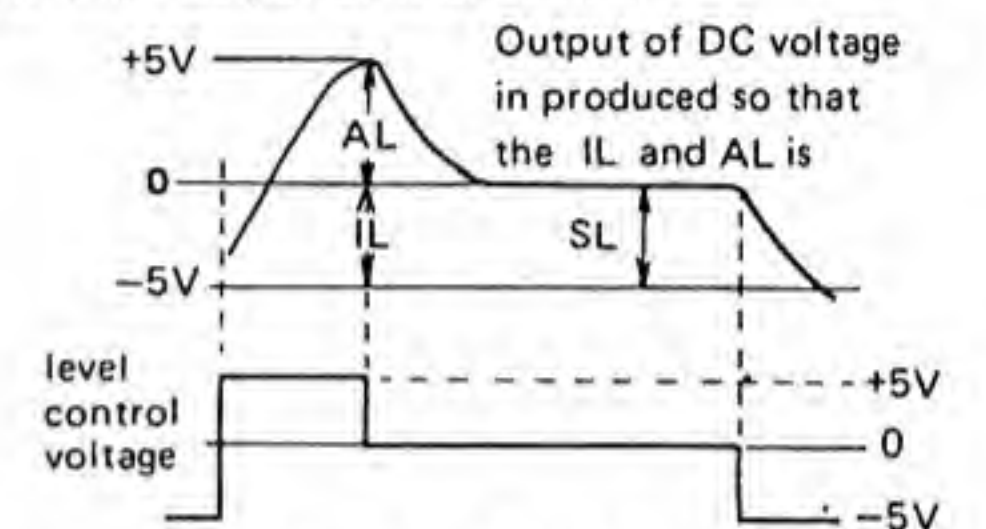


12. TC Output of the time control.
Output of DC voltage is produced so that the each time of attack, DT and RT are controlled.



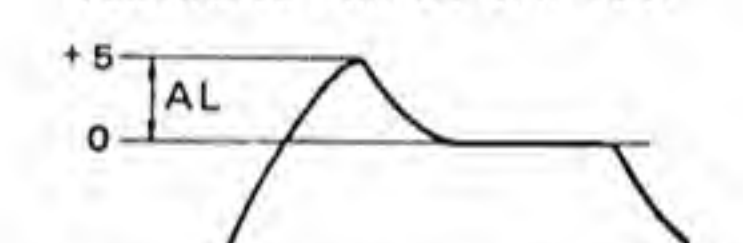
The higher the voltage, the shorter the time and the lower the voltage the longer the time.

13. LC Output of level control.

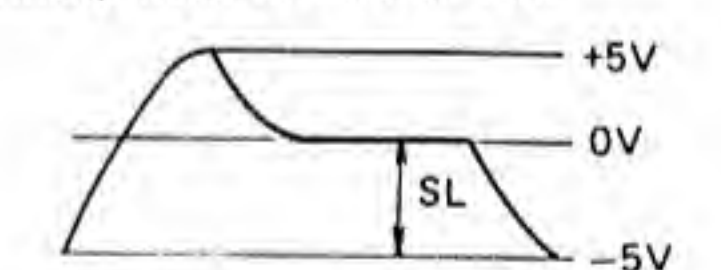


The higher the voltage, the higher the level and the lower the voltage the lower the level.

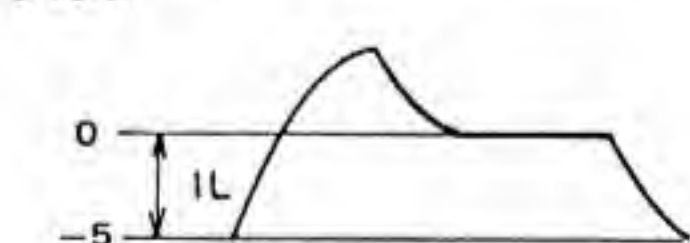
14. AL Input of buffer voltage for determination of attack level.
Input of the voltage between (0V~10V) is provided and the attack level is controlled from 0V until +5V.



15. SL Input of buffer voltage for determination of the sustain level.
Normally fixed to zero(0) volt.



16. IL Input of buffer voltage for determination of the initial level.
Input of the voltage between zero 0V and ten 10V is provided and the initial level is controlled from zero to minus 5 volt.

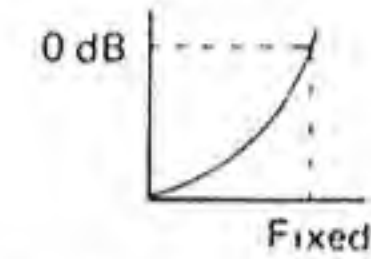


← Explanation for IC
(IC 説明)

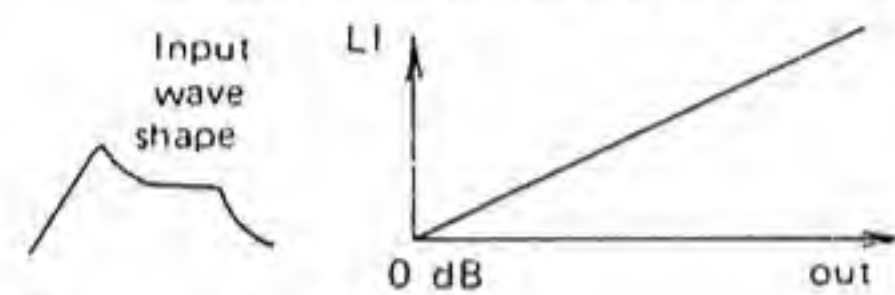
VCA Circuit Diagram

VCA IC (IG00151)

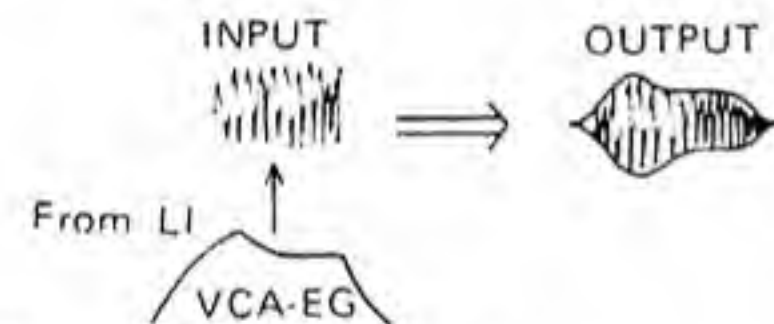
1. EI Input voltage for level control.
Input of the control voltage is provided for changing the level exponentially.



2. LI Input of level control voltage.
Input of the control voltage is provided for linear change of the level.



3. +IN Input
Input of the level modulated signal is provided.

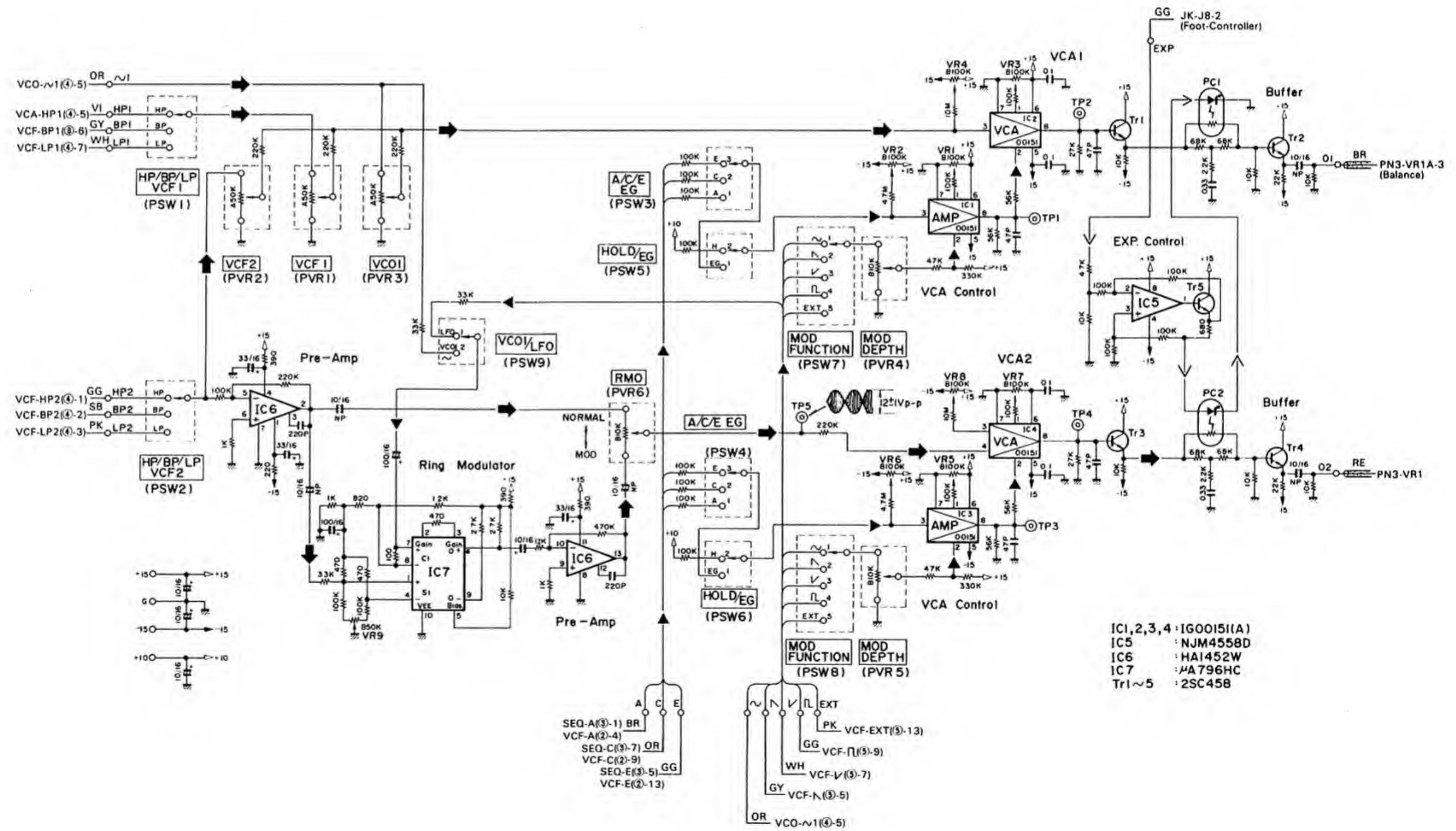
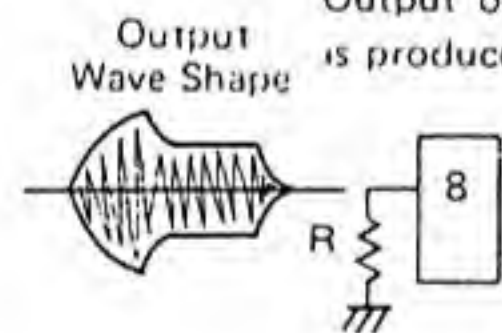


4. -IN Negative feed back.
Normally unused.

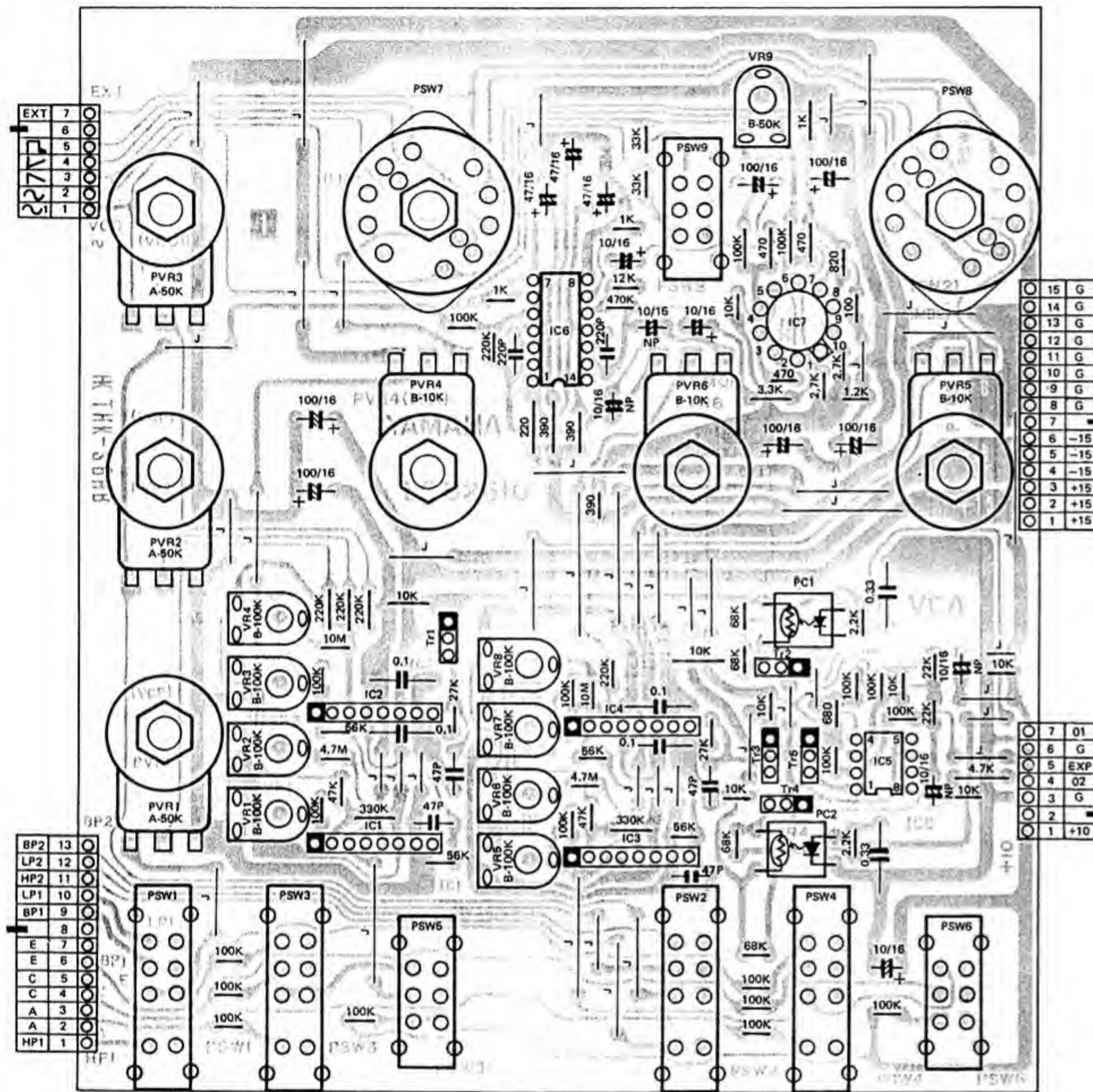
5. Vee -15V input power source.
6. Vcc +15V input power source.

7. GND Earth
8. OUT Output

Output of the following wave shape is produced.



VCA Circuit Board & Wiring



View from the printed pattern side of the circuit board.
パターン側から見た部品配置です。

(Note)

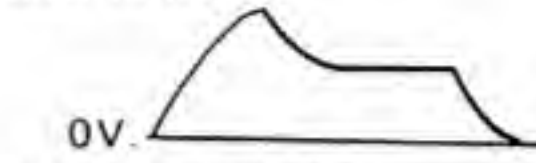
1. IC
 IC1 ~ 4 : IG00151
 IC5 : NJM4558
 IC6 : HA1452
 IC7 : μ A796HC
2. Transistor (トランジスタ)
 Tr1 ~ 5 : 2SC458
3. Photo coupler
 PC1 · 2 : P558-G50-201B
4. Semi Variable Resistor (半固定抵抗)
 UR1 ~ 9 : V8K-4-1 Type

VCA-EG IC (IG00159)

This IC generates envelope wave shape which is supplied to VCA and control the tone volume.

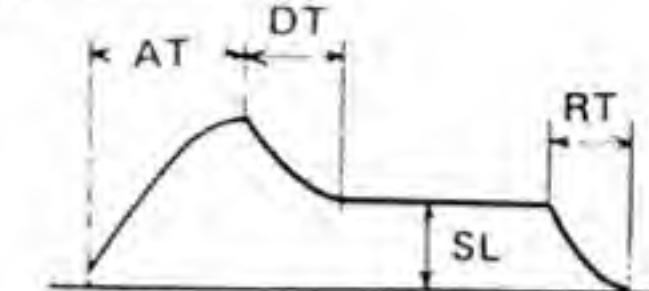
1. IL Input of initial level.

Fixed to 0V



2. BI Input of buffer amplifier.

3. OUT The buffer amplifier is built in for the purpose of matching impedance.
Output wave shape

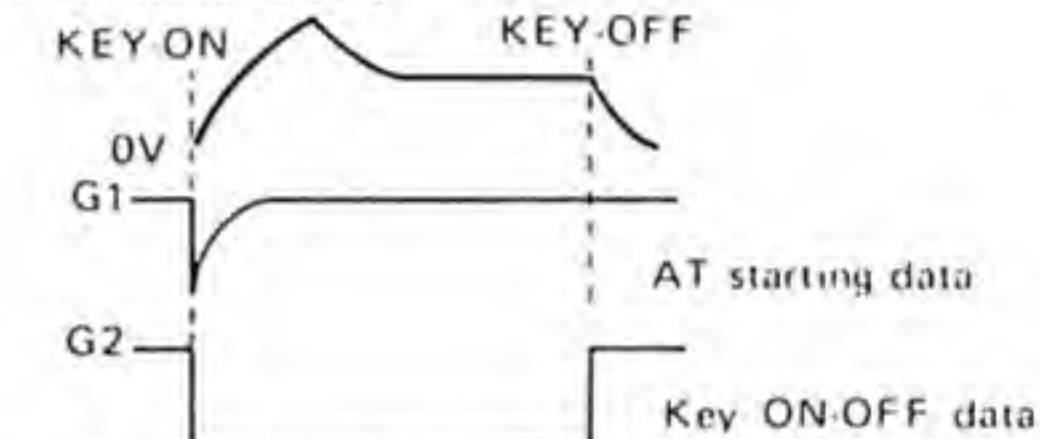


4. GND Earth

5. Vcc +15V input power source.

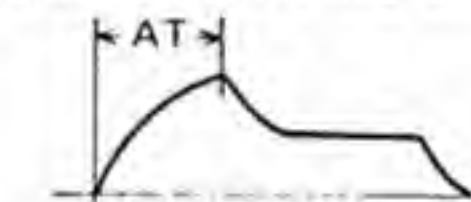
6. G1 Gate 1

7. G2 Gate 2

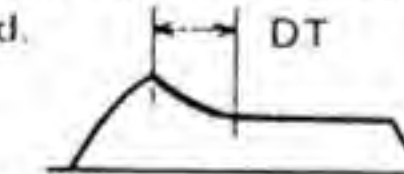


8. Vee +15V input power source.

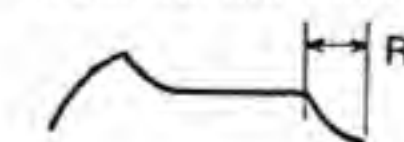
9. AT Input of buffer voltage for determination of attack time.
Input of the voltage between zero V and 10V is provided and the attack time is controlled from 1 mS until 1S.



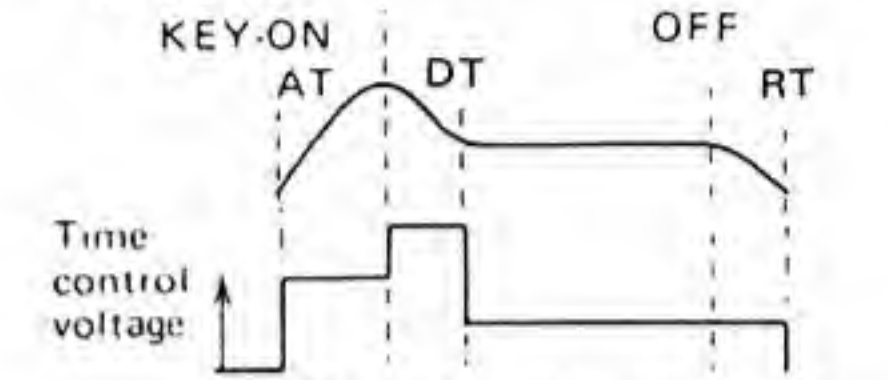
10. 1DT Input of buffer voltage for determination of decay time.
Input of the voltage between zero V and 10V is provided and the decay time is controlled from 10 m second until 10 second.



11. 2DT Input of buffer voltage for determination of release time.
Input of the voltage between zero V and 10V is provided and the time key-off until release is controlled from 10 mS until 10 S.

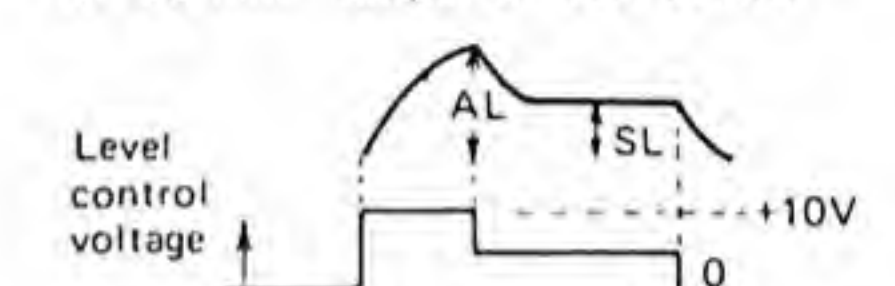


12. TC Output of time control.
Output of the DC voltage is produced so that the each time of Attack, 1st Decay and 2nd Decay are controlled.



The higher the voltage, the shorter the time and the lower the voltage, the longer the time.

13. LC Output of level control

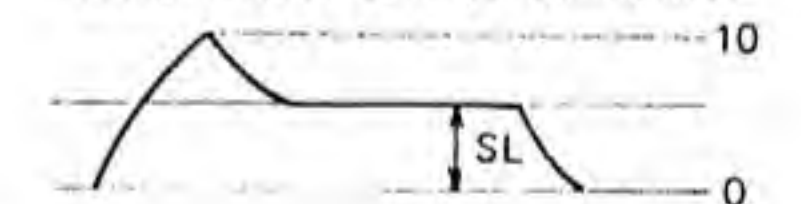


Output of the DC voltage for AL and SL control is provided.

The higher the voltage, the higher the level and the lower the voltage, the lower the level.

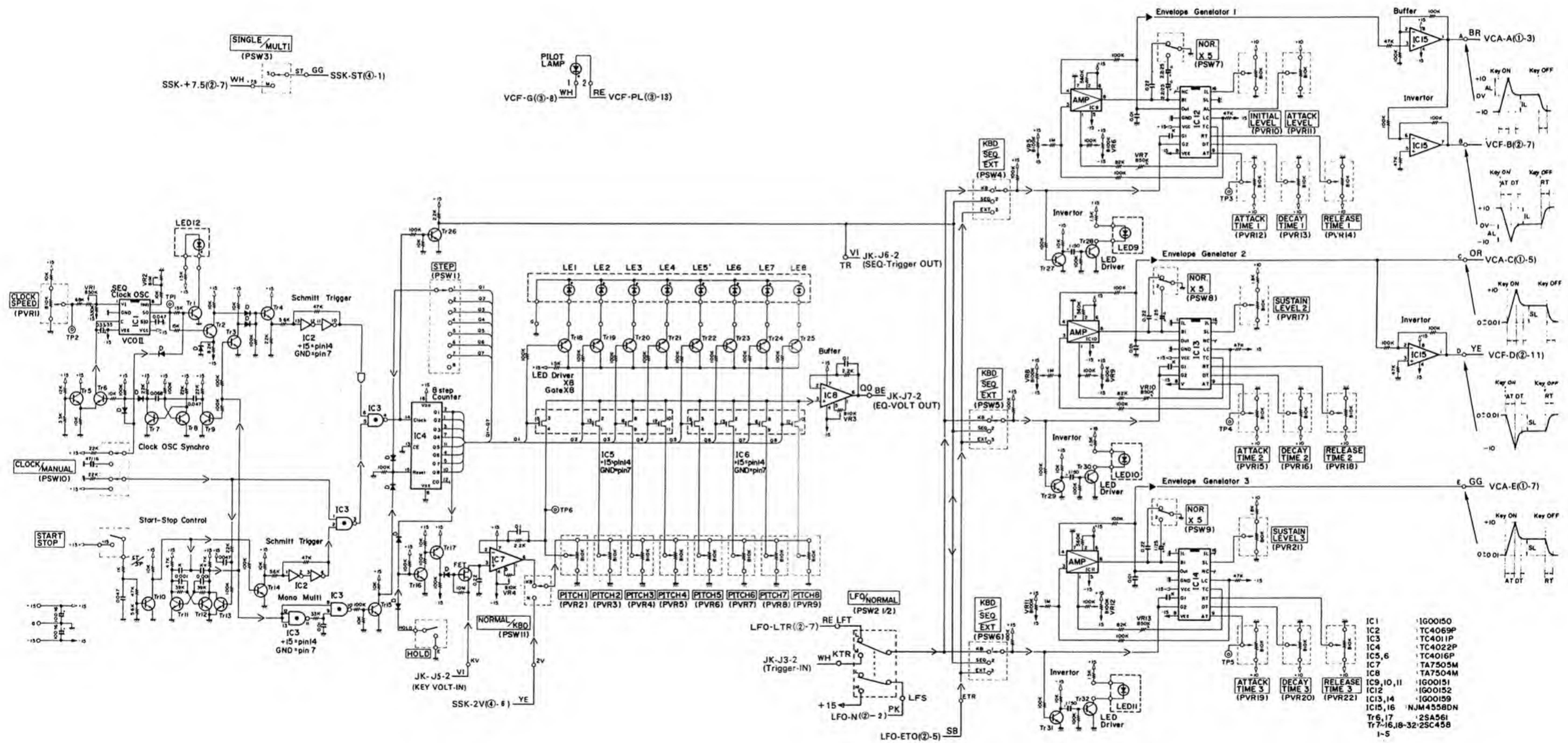
14. NC Not connected.

15. SL Input of buffer voltage for determination of the sustain level.
Input of the voltage between zero V and 10V is provided so that the sustain level can be controlled.



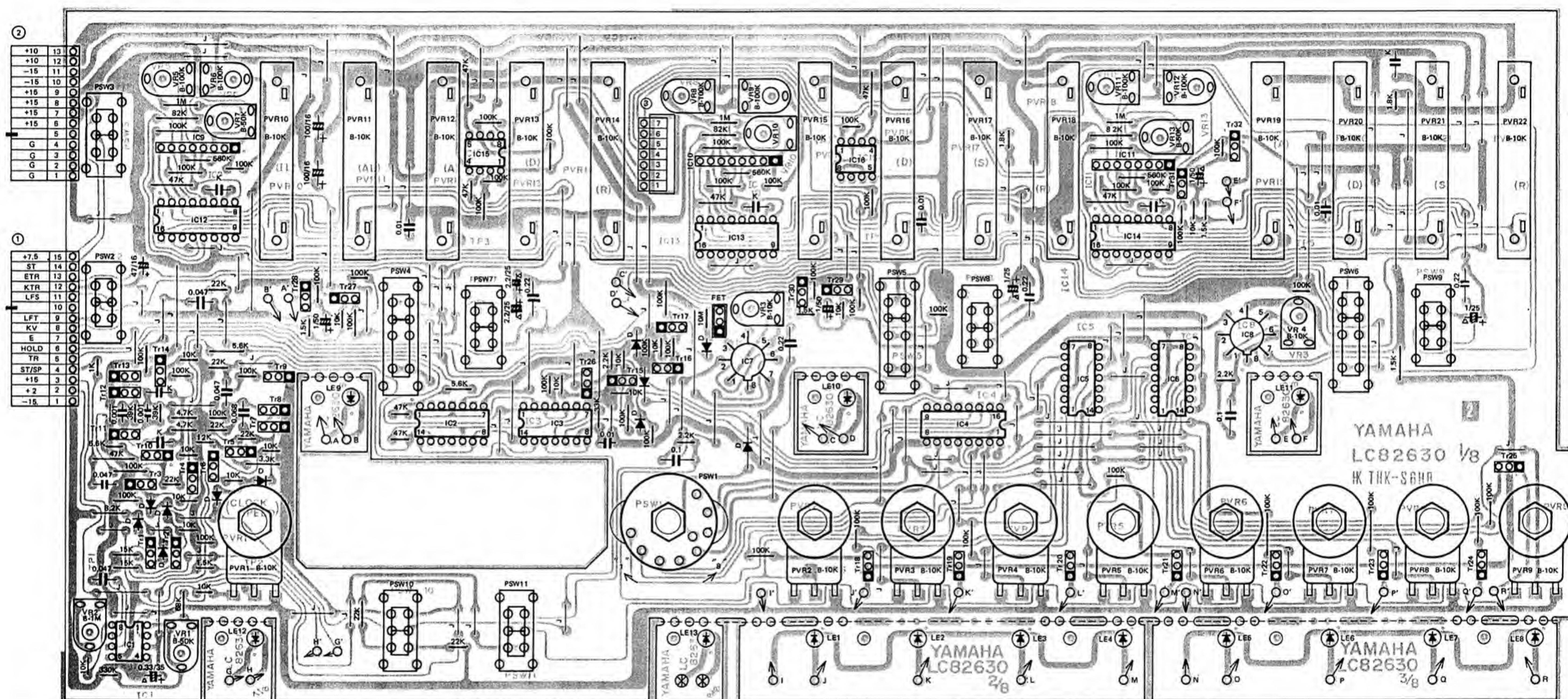
16. NC Not connected.

SEQ Circuit Diagram



SEQ Circuit Board & Wiring

7	C
6	D
5	E
4	F
3	G
2	H
1	A

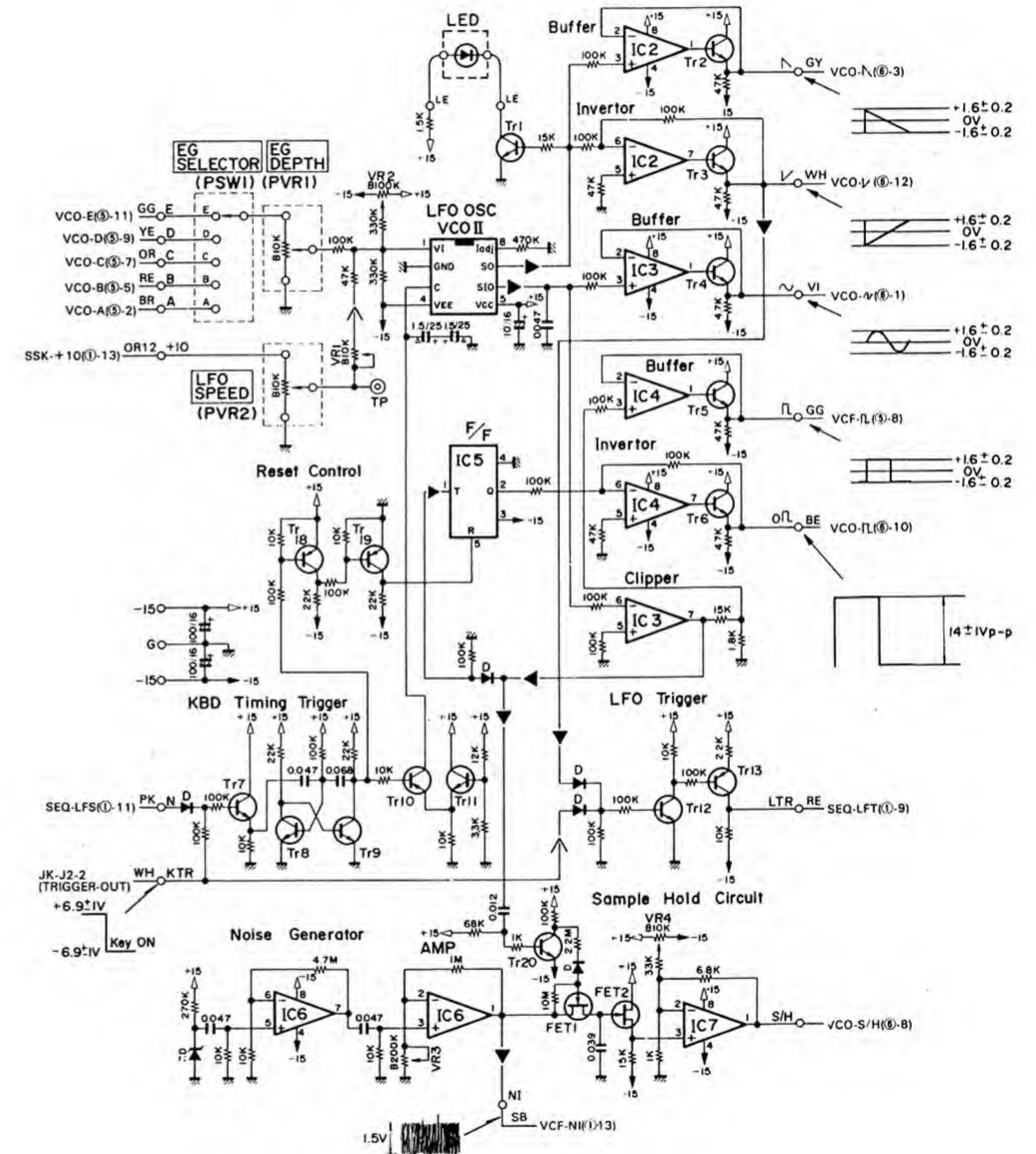
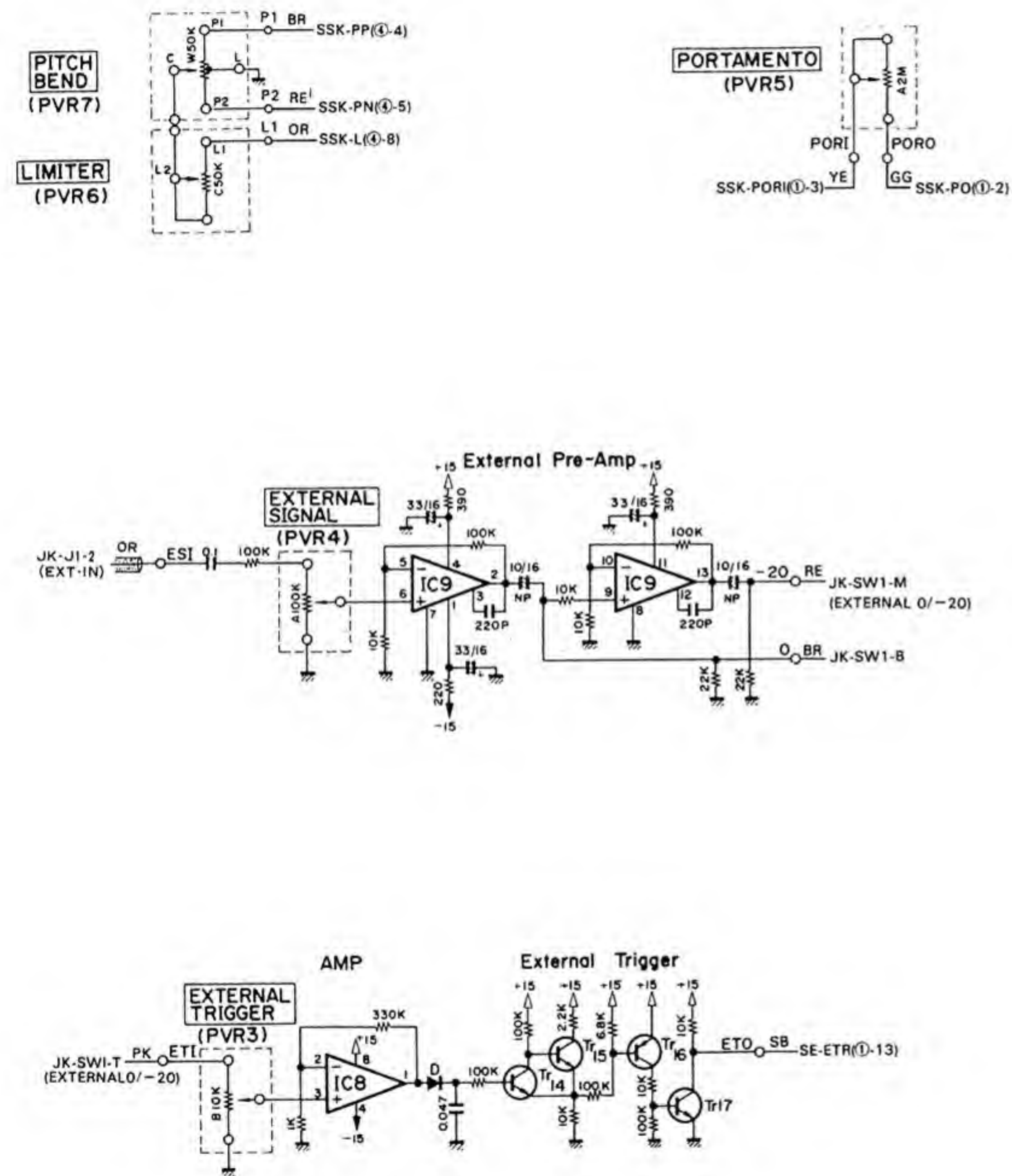


View from the printed pattern side of the circuit board.
パターン側から見た部品配置です。

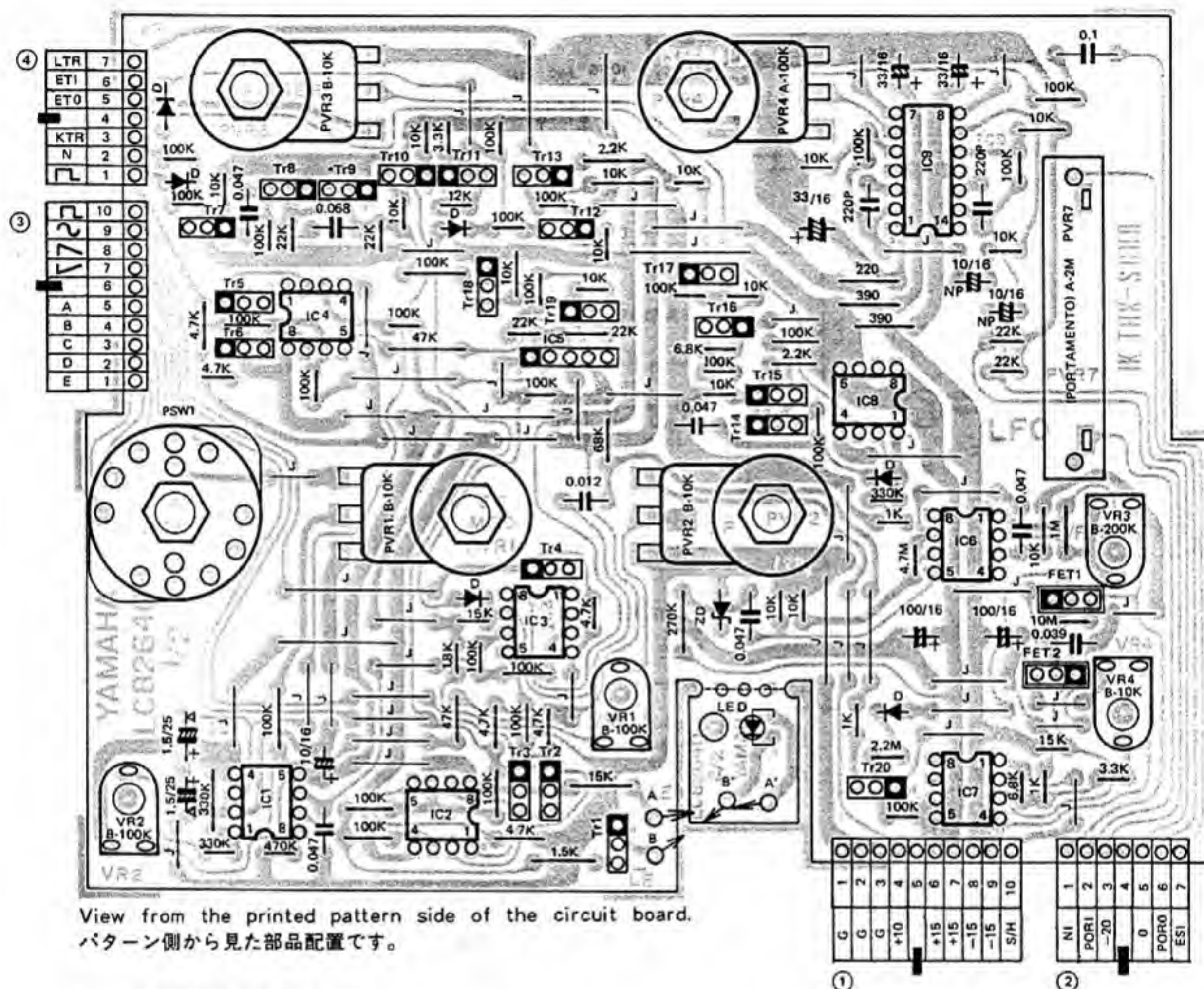
(Note)

- | | | | |
|---------|-----------|------------------------|----------|
| 1. IC | | 2. Transistor (トランジスタ) | |
| IC1 | : IG00150 | Tr6,17 | : 2SA561 |
| IC2 | : TC4069P | other | : 2SC458 |
| IC3 | : TC4011P | 3. FET | : 2SK30A |
| IC4 | : TC4022P | 4. Diode (ダイオード) | |
| IC5,6 | : TC4016P | D | : 1S1555 |
| IC8 | : TA7504M | 5. LED (発光ダイオード) | |
| IC9~11 | : IG00151 | SLP1328 | |
| IC12 | : IG00152 | | |
| IC13,14 | : IG00159 | | |
| IC15,16 | : NJM4558 | | |
| IC7 | : TA7505M | | |

LFO Circuit Diagram

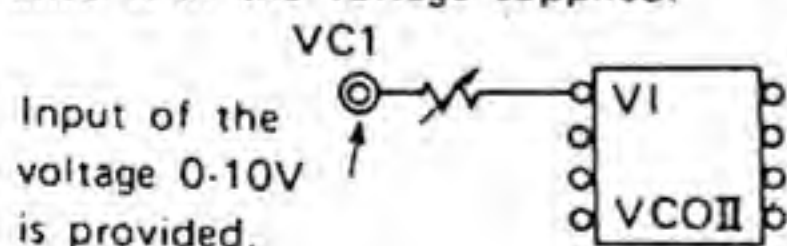


LFO Circuit Board & Wiring

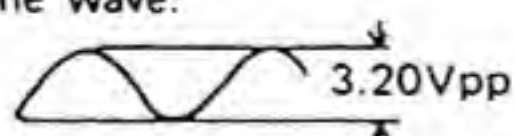


VCO II (IG00150)

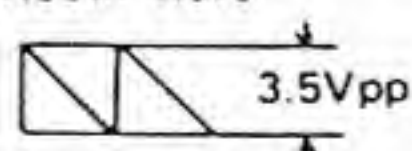
1. VI Input of the control voltage.
The frequency is variable in accordance with the voltage supplied.



2. GND Earth
3. C Capacitor for determination of the frequency.
4. Vee -15V input power source.
5. Vcc +15V input power source.
6. SIO Output of sine wave.



7. SO Output of sawtooth wave

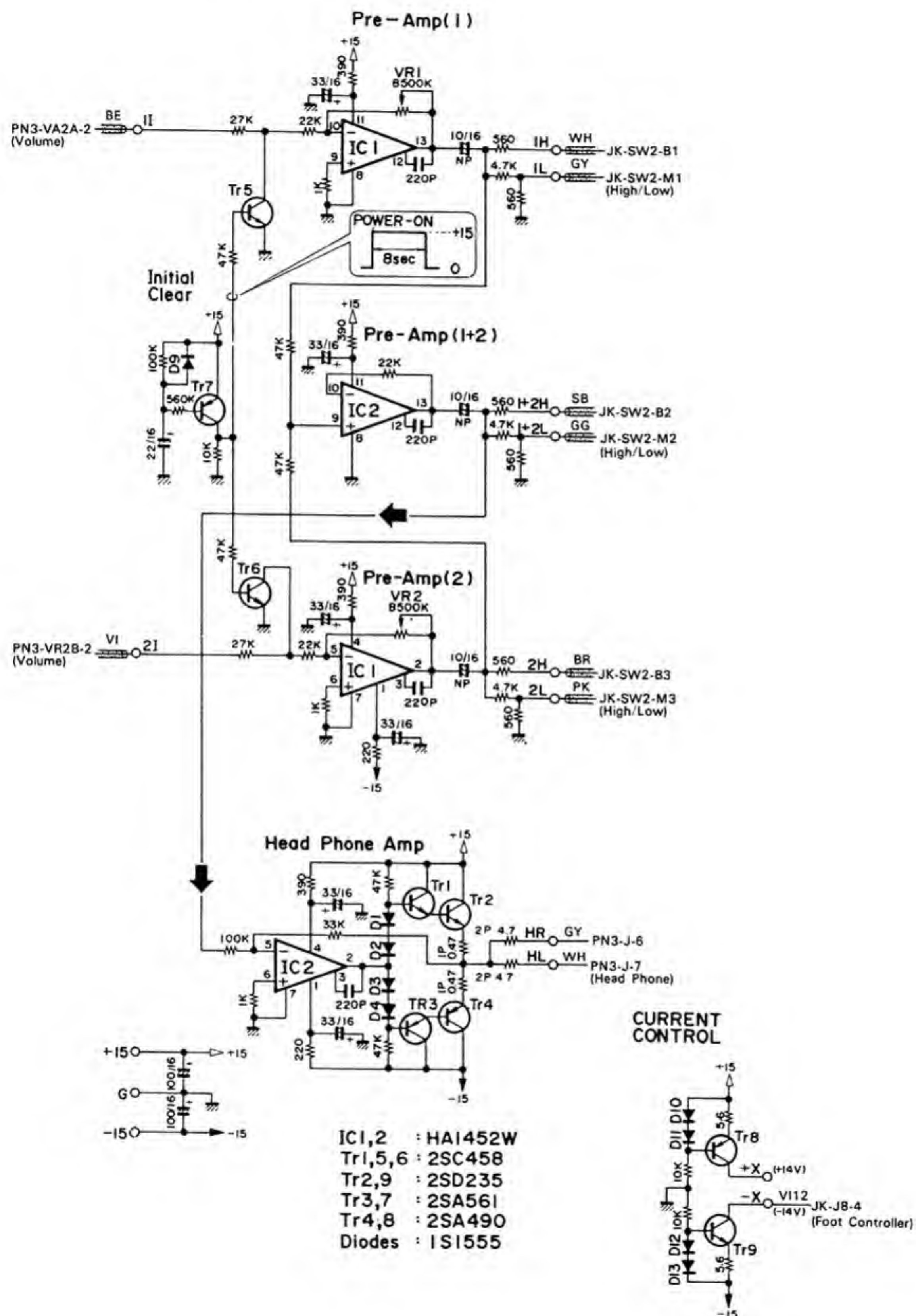


8. Iadj Setting for standard electric current.

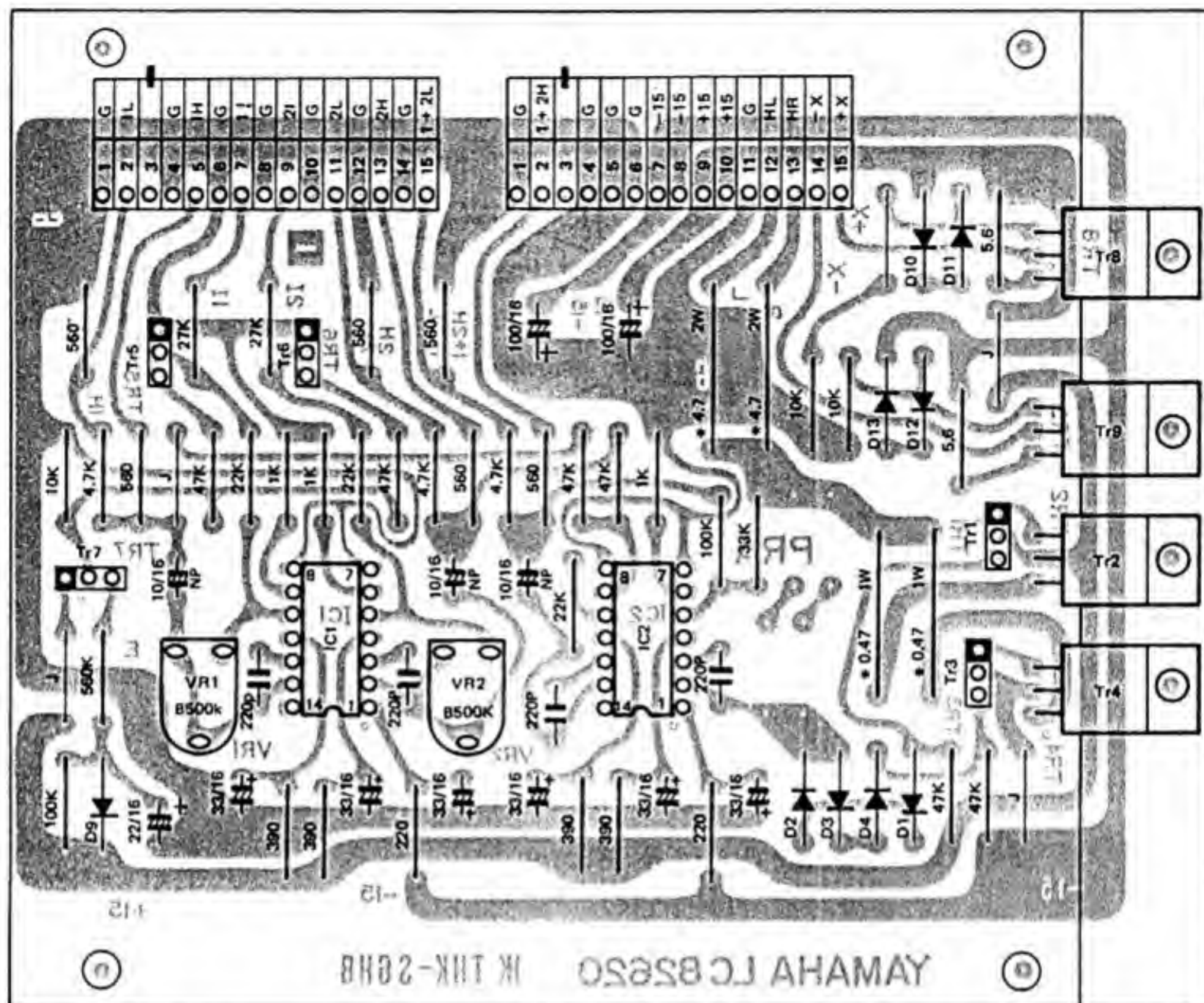
- (Note)

1. IC
IC1 : IG00150
IC5 : BA634
IC9 : HA1452
IC2 ~ 4, 6 ~ 8 : NJM4558
2. Transistor (トランジスタ)
Tr1 ~ 9, 11, 12, 14, 15, 17, 20 : 2SC458
Tr10, 13, 16, 18, 19 : 2SA561
3. Diode (ダイオード)
D : 1S1555
ZD : 1S1715
4. FET
FET1, 2 : 2SK30A

PRA Circuit Diagram

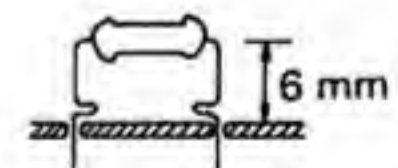


PRA Circuit Board & Wiring

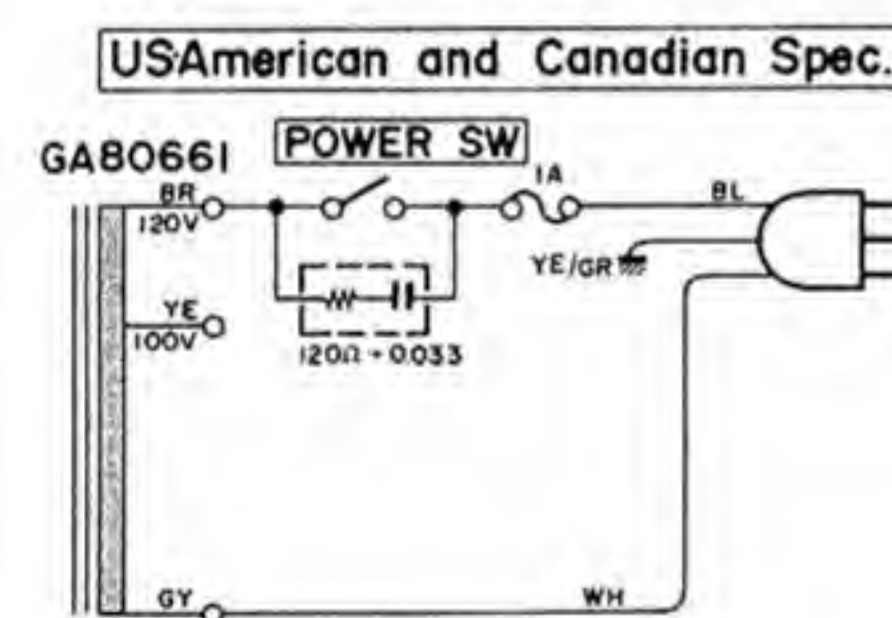
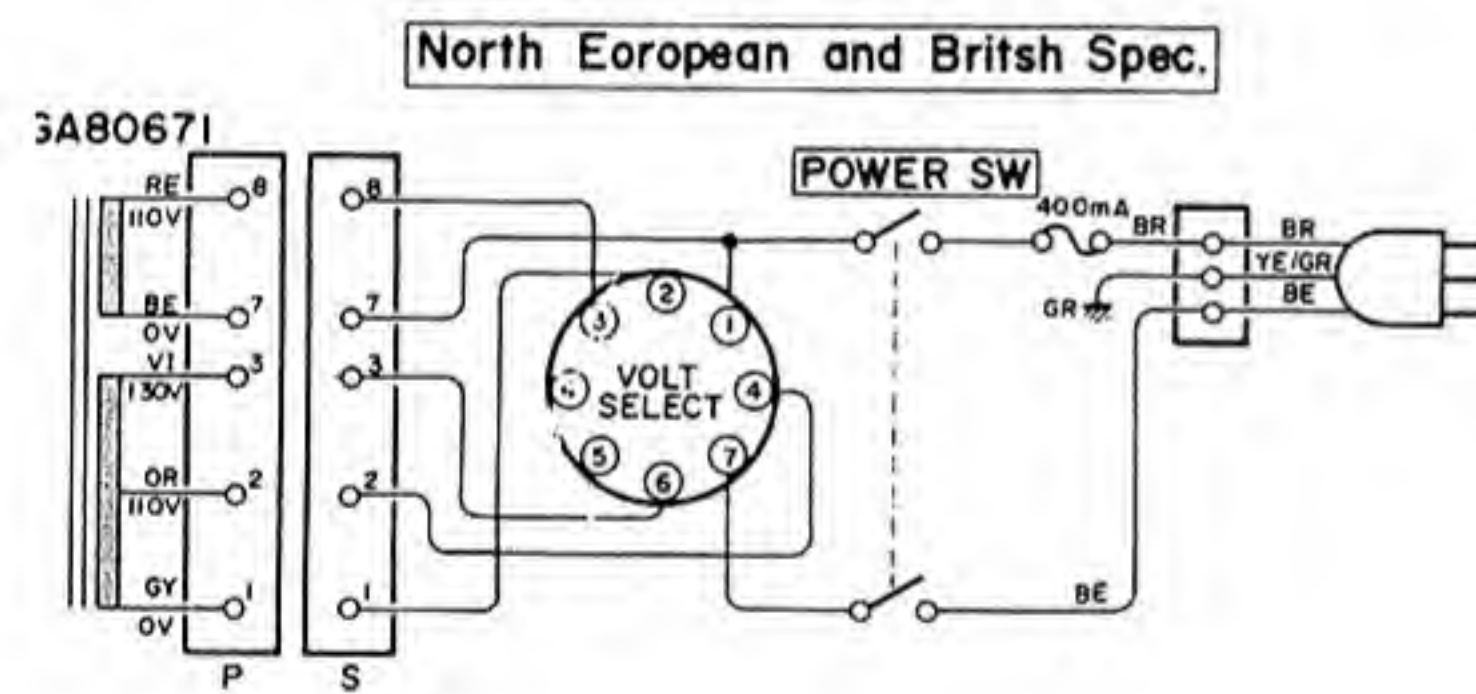
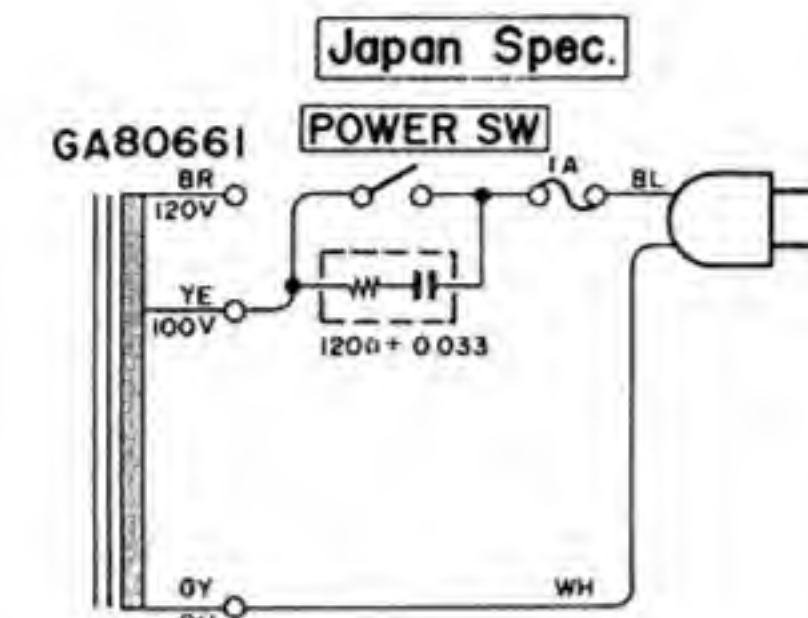
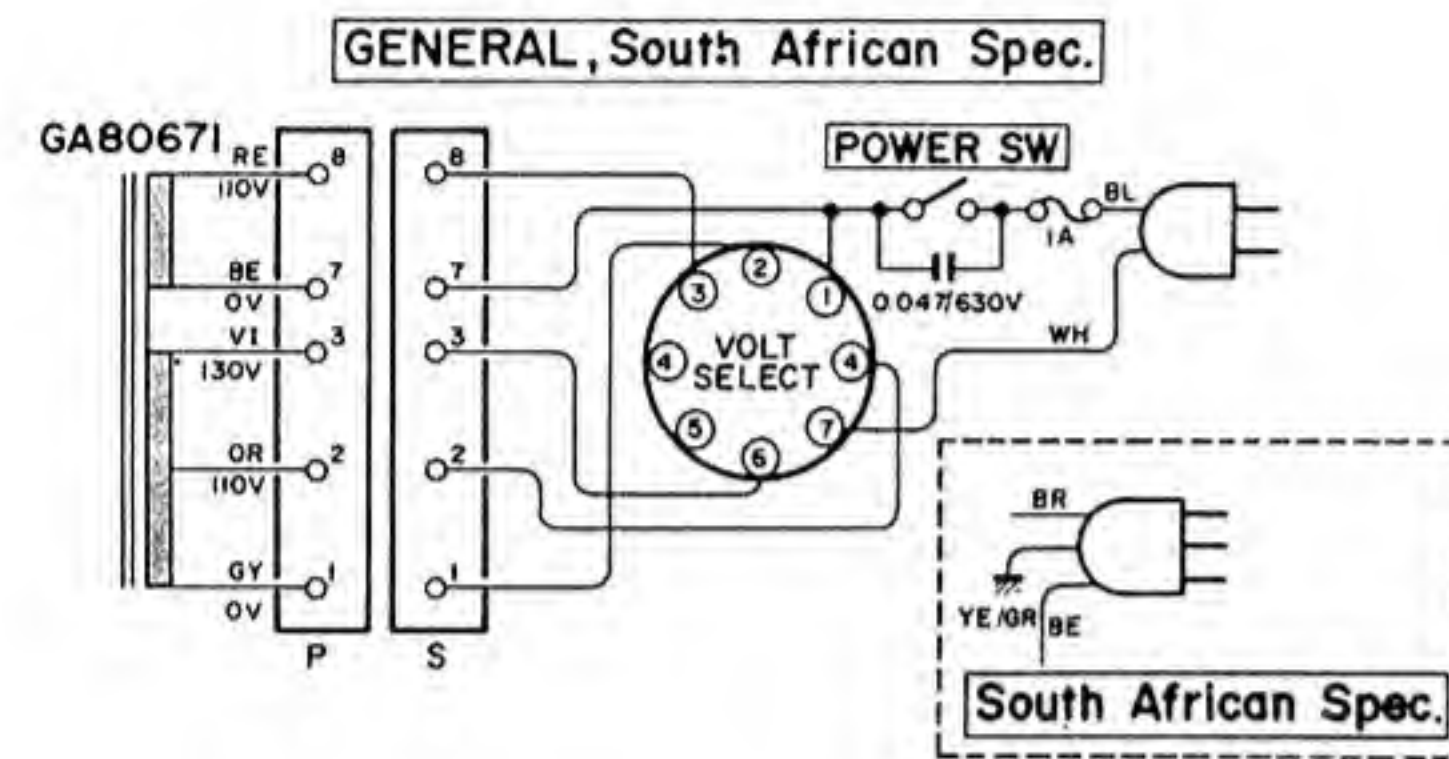


(Note)

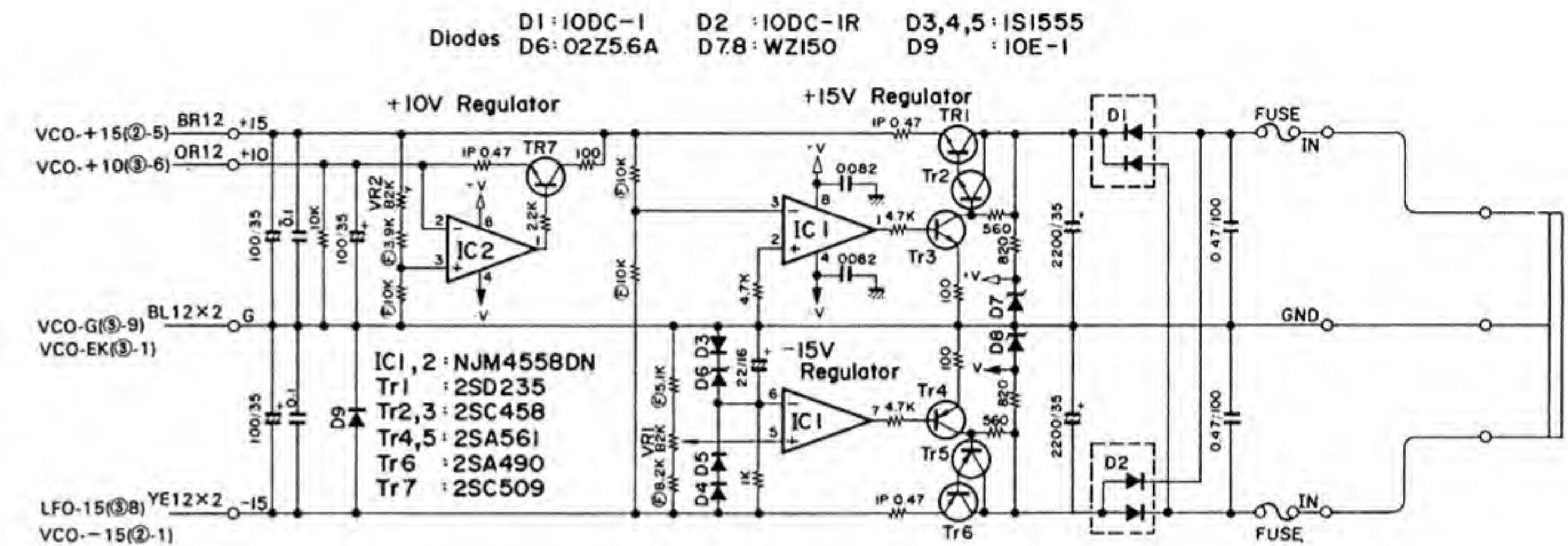
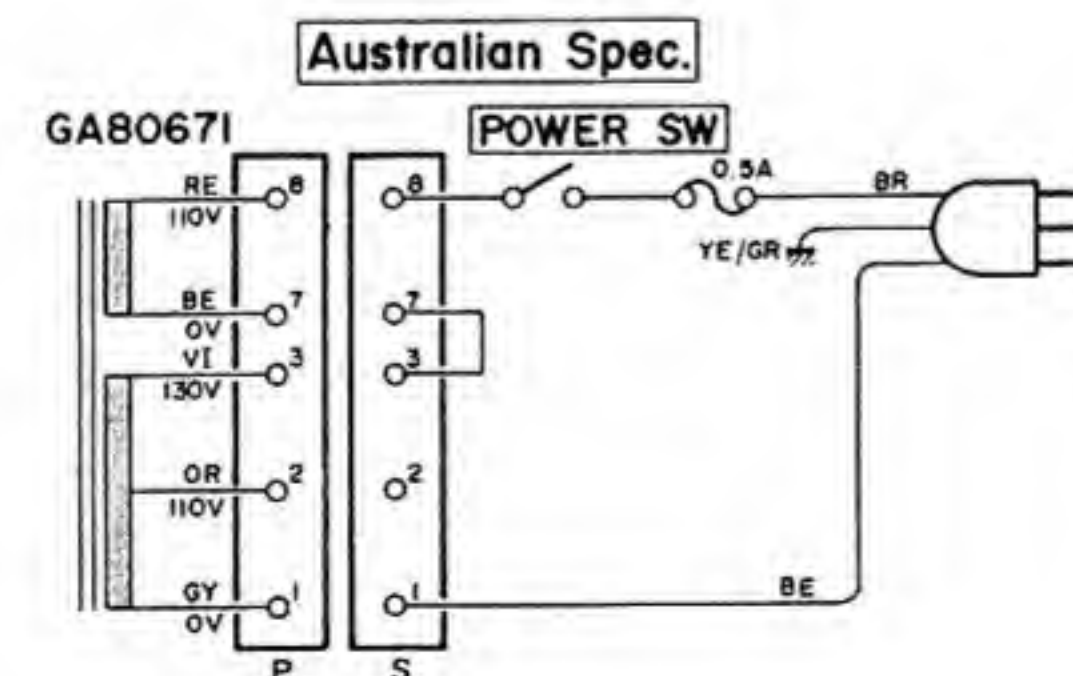
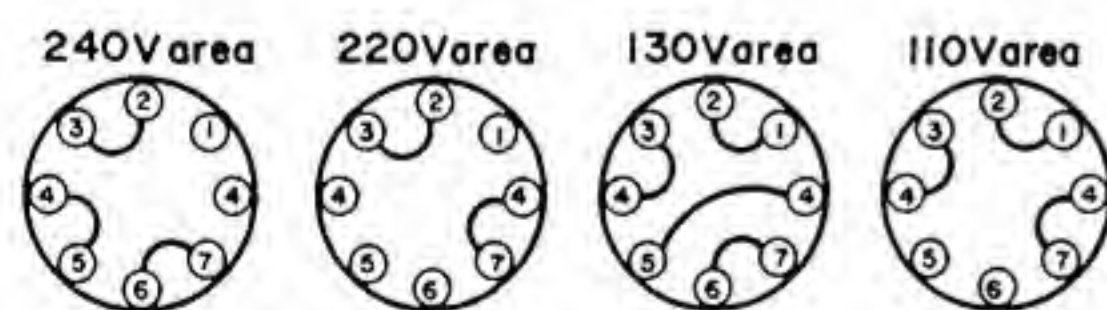
1. IC
IC1,2 : HA1452
2. Transistor (トランジスタ)
Tr1,5,6 : 2SC458
Tr2,9 : 2SD235
Tr3,7 : 2SA561
Tr4,8 : 2SA490
3. Diode (ダイオード)
D1 ~ 13 : 1S1555
4. Semi Variable Resistor (半固定抵抗)
VR1,2 : V8K-4-1
5. Metal oxide film resistor (酸化金抵抗)
* marks:



ADC Circuit Diagram

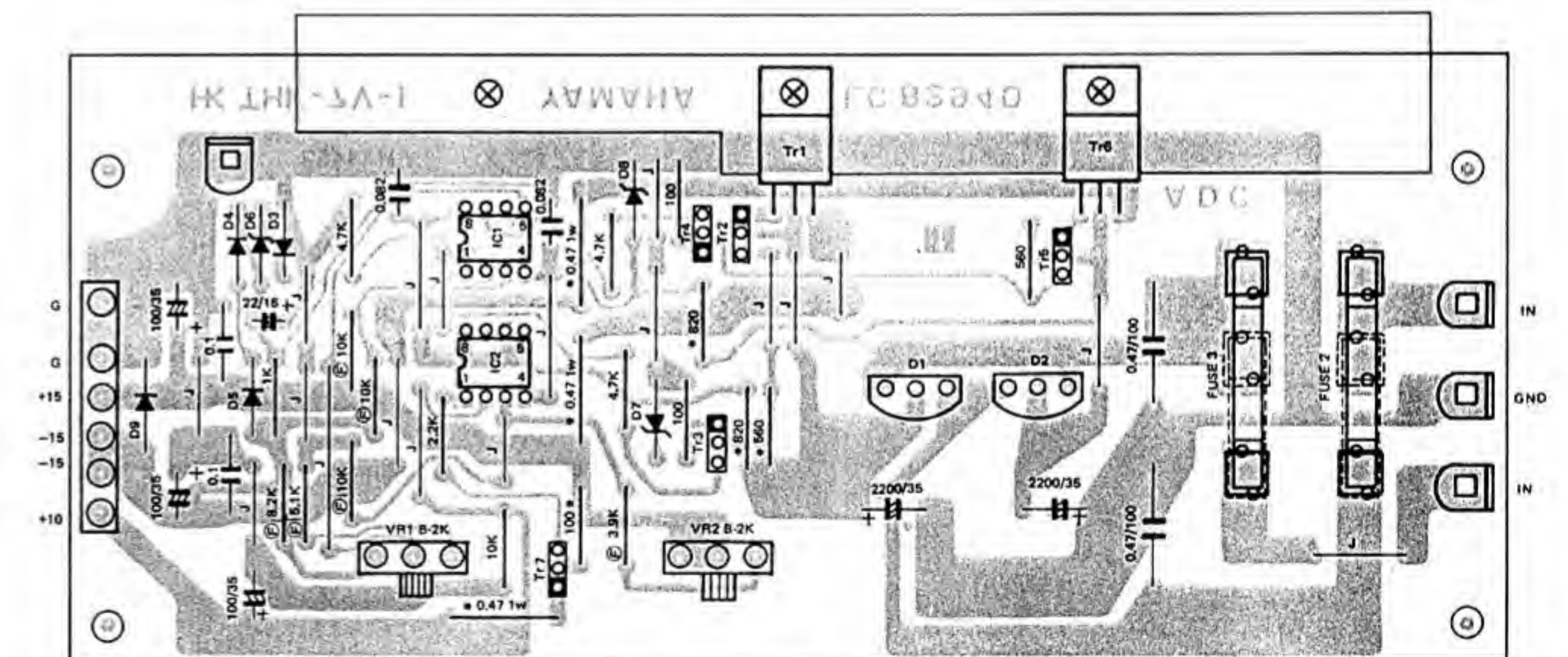


ACTUAL CONNECTIONS ON VOLTAGE SELECTOR



KEC-10114-77A

ADC Circuit Board & Wiring



(Note)

1. FUSE 2-3

- | | |
|--------------------|---------------|
| Japan | 1.5 AT |
| N.European, BS ... | 1.6 AT (mini) |
| other | 1.5 AT (UL) |

- ## 2. Transistor (トランジスタ)

- Tr1 : 2SD235

- Tr2,3 : 2SC458

- Tr4,5 : 2SA561

- Tr6 : 2SA490

- Tr7 : 2SC509

- ### 3. Diode

- D1 : 10DC-1

- i) D2 : 10DC-1R

- D3,4,5 : 1S1555

- D6 : 02Z5.6A

- D7,8 : WZ150

- D9 : 10E-1

4. IC

- IC1,2 : NJM4558

- 101,2 1.150.000

- ### 5. Resistor (抵抗)

- mark : 1%

- 0.47Ω 1W : Met

- ```
* mark :
```

- III

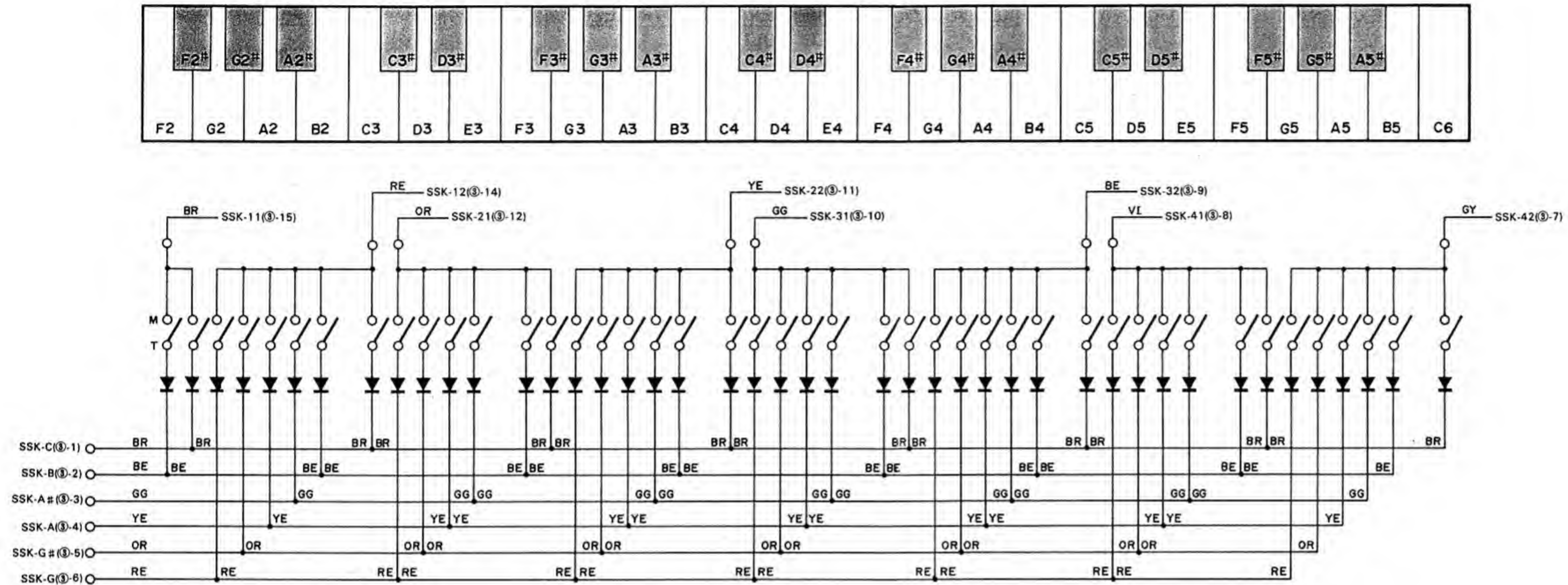
- 12

6. Semi variable resi

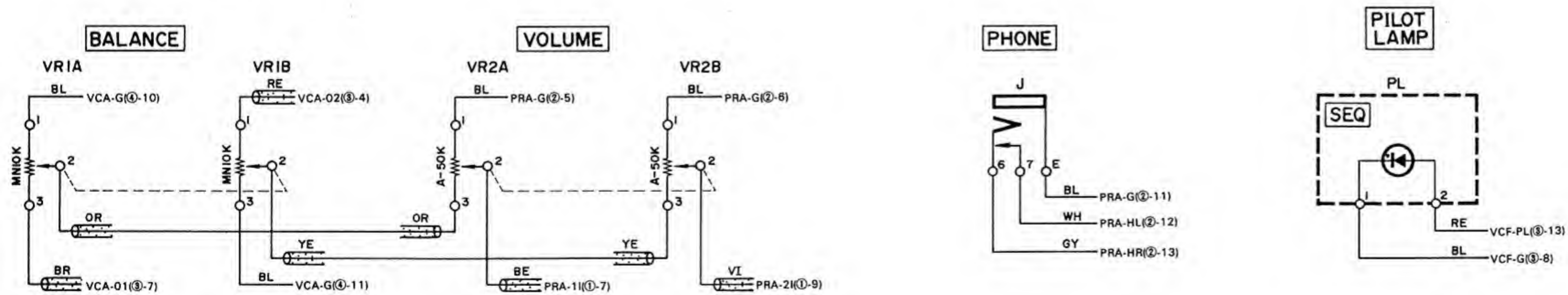
- RV1.2 : V18

- TABLE 1



**KEY SWITCH** Circuit Diagram

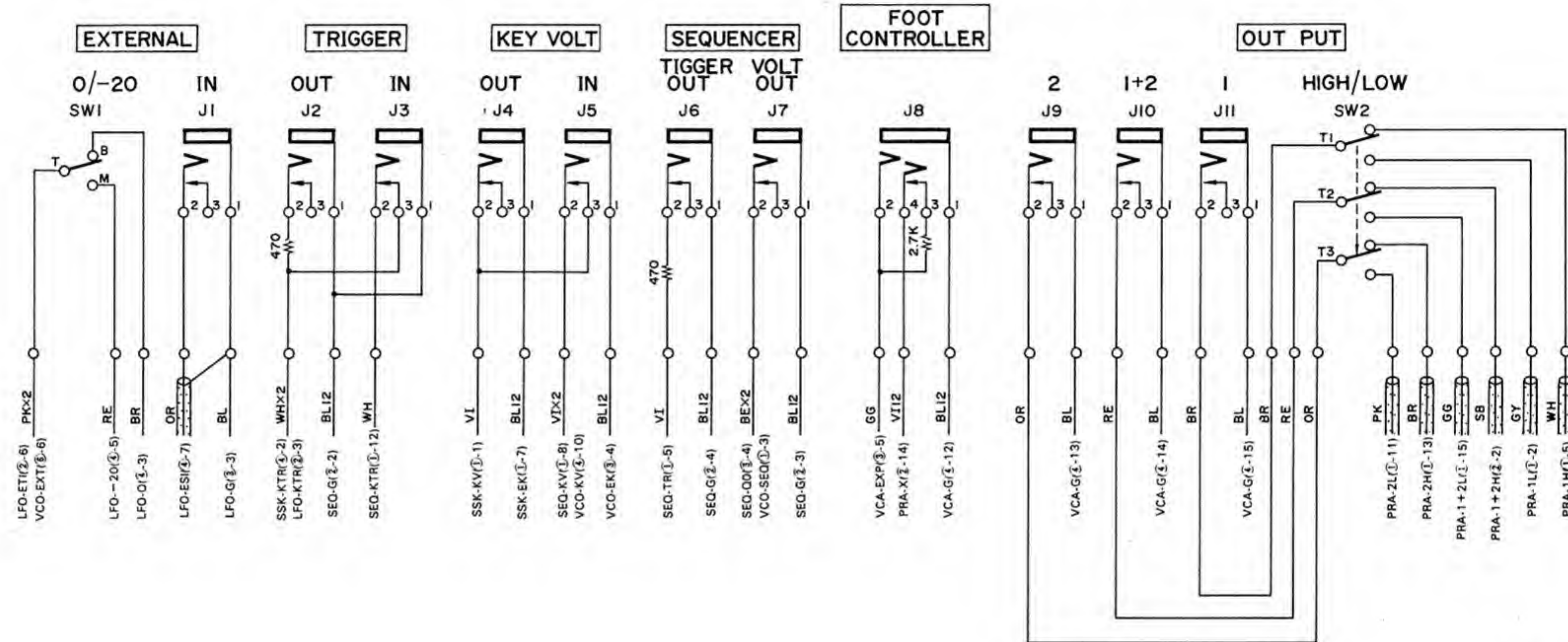
KEC-90113-78△

**PN3** Circuit Diagram

KEC-90113-78△

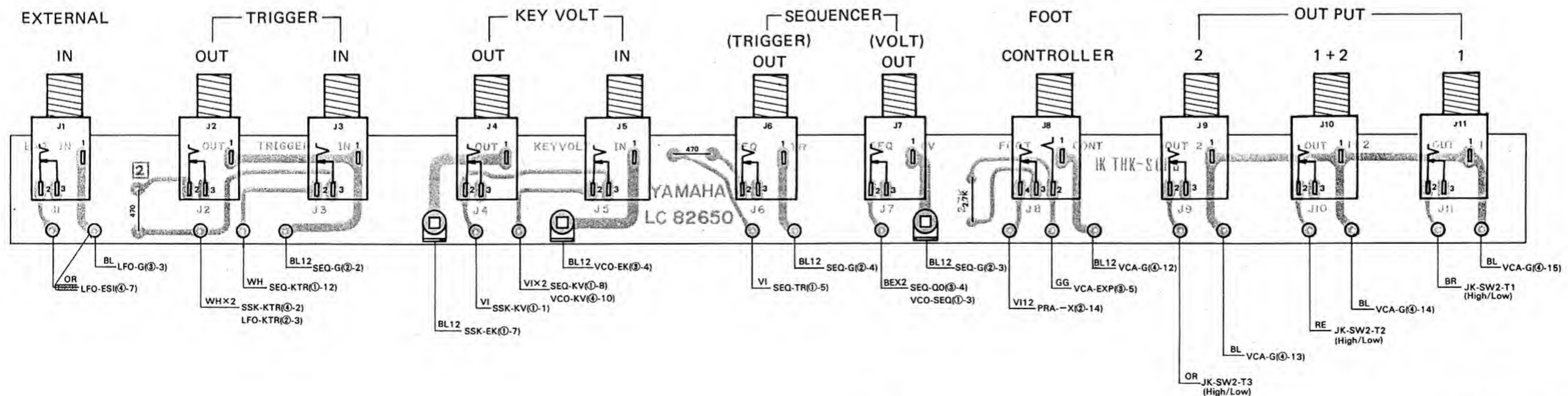


# **REAR PANEL** Circuit Diagram (JK)



KEC-90113-78 Δ

# **REAR PANEL** Circuit Board & Wiring





## Standard for circuit inspection and adjustment

### ADC Circuit Board

#### 1. -15V Adjustment (+15V Adjustment)

Adjust **VR1** until a voltage of  $-15.00\text{V}$  is present across  $-15\text{V}$  and E terminals. Then, make sure that a voltage of  $+15 \pm 0.15\text{V}$  is present across  $+15\text{V}$  and E terminals.

#### 2. +10V Adjustment

Adjust **VR2** until a voltage of  $+10.00\text{V}$  is present across  $+10\text{V}$  and E terminals.

#### 3. Load Characteristics

When no load is applied, the fluctuation should be smaller than  $\pm 0.5\%$  and should show neither oscillation nor abnormal voltage.

Make sure that the regulator's response to load fluctuation is within 50m sec. When connecting Mylar capacitors of  $0.47\mu\text{F}$  across each terminal and the E terminal, make sure that neither oscillation nor abnormal voltage is generated and the response time is within 50m sec.

#### 4. First Stage Voltage and Output Voltage

When load is fully applied, the output voltage fluctuation should be smaller than  $\pm 0.1\%$  for the first stage voltage fluctuation of  $\pm 15\%$ , and the regulator should respond within 50m sec to a drastic change in the first stage voltage.

#### 5. Ripple Noise

When load is fully applied, make sure that ripple noise smaller than  $10\text{mVp-p}$  is present at each output terminal.



## SSK Circuit Board

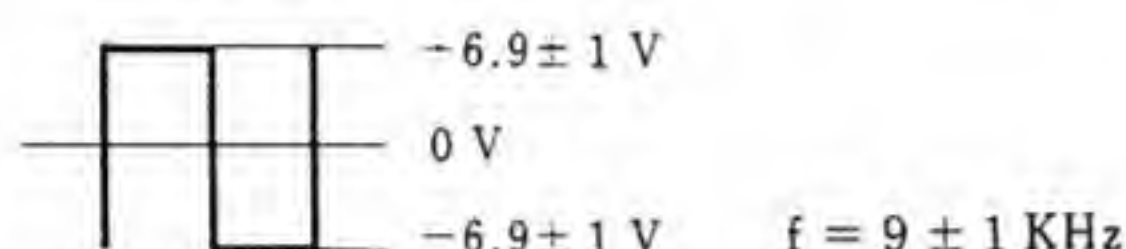
### 1. Power Supply for Key Assignor

+7V Adjustment . . . . . Make sure that voltage of  $+6.9 \pm 0.6\text{V}$  is present at 1st Pin of IC<sub>1</sub>.

−7V Adjustment . . . . . Make sure that voltage of  $-6.9 \pm 0.6\text{V}$  is present at 40th Pin of IC<sub>1</sub>.

### 2. Key Assignor Clock

Make sure that a waveform as in the figure below is obtainable at 2nd Pin of IC<sub>2</sub>.



### 3. Pitch Bend Voltage Generator Circuit

a. Set the PITCH BEND knob to 0 position, then adjust **VR 4** until 2.000V is obtained at CP6 or 2V (④−6.7) terminal.

b. Set the LIMITTER lever to MAX position and PITCH BEND knob to “+” position, then adjust **VR 6** so that 4.000V is obtained at PB (④−13) terminal.

**Note:** When PITCH BEND knob is in “−” position 1.00V is obtained at PB terminal.

### 4. Key Voltage Modulator Circuit

a. Set the PITCH BEND knob to 0 position, then adjust **VR 5** so that −2.000V is obtained at CP7.

b. Adjust the TUNE knob until 0.000V is present at TU (④−10) terminal. Set the EG−DEPTH knob in PITCH Section to 0 position, then adjust **VR 3** so that 2.000V is obtained at CP8.

### 5. Key Voltage Generator Circuit

a. Press F<sub>2</sub> key and adjust **VR 7** so that  $250 \pm 0.2\text{mV}$  is obtained at CP9.

b. After the item 4−(a) adjustment, adjust **VR 1** so that  $166.8 \pm 0.1\text{mV}$  is obtained at CP10 or PI (①−3) terminal.

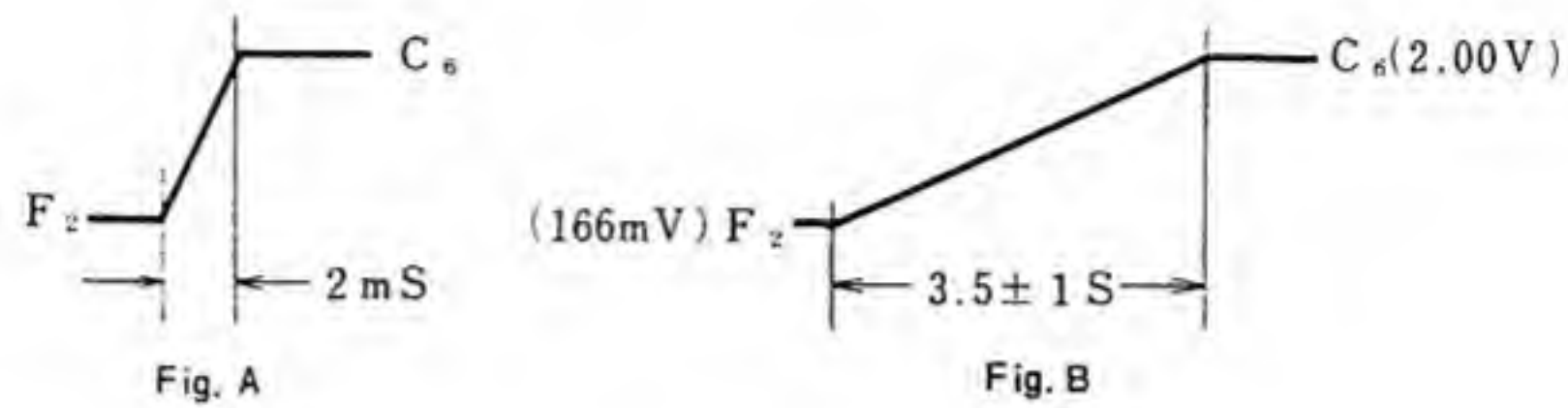
c. After the item 4−(b) adjustment, adjust **VR 2** until  $166.8 \pm 0.1\text{mV}$  is present at CP11 or KV (①−1) terminal.

### 6. Portamento Circuit

a. Set the PORTAMENTO lever to S position, press F<sub>2</sub> key, and then turn C<sub>6</sub> key on, make sure that a waveform as in the figure A is obtainable at KV (①−1) terminal.

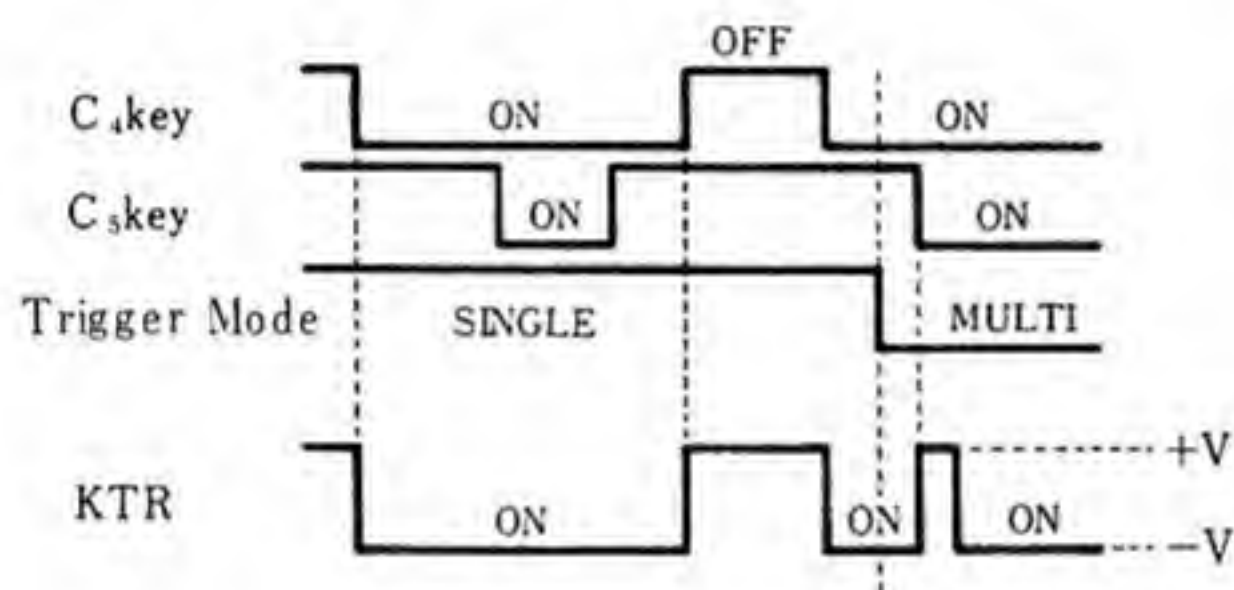
b. Set the PORTAMENTO lever to L position, then make sure that a waveform as in the figure B is obtainable at the same.





### 7. Trigger Mode Convertor Circuit

Turn on and off the  $C_4$  and  $C_5$  keys as in the figure below, change the key mode from SINGLE to MULTI, and make sure that the KTR terminal output is as shown in the figure.



During SINGLE Mode, as long as a key remains depressed, operating other keys has no effect on the KTR, which is kept ON.

During MULTI Mode, depressing keys successively permits KTR to turn ON one after another with priority given to higher tones.



## VCO Circuit Board

### 1. Tune Circuit

Set the TUNE knob to fully [–] position and [+] position, make sure that  $+75 \pm 5\text{mV}$  and  $-75 \pm 5\text{mV}$  are respectively obtainable at TU (①–1) terminal.

### 2. EG Modulator Circuit

Set the SEQ/KBD/EXT switch in Envelope Generator 2 to KBD position, AT, DT, RT to S, SL to 10, EG–SELECTOR (PSW1) to C position, EG–DEPTH (PVR3) to 10 and turn a key ON, make sure that 0.8V is obtainable at EG (⑤–13) terminal. (+8V Envelope voltage waveform is fed into C (⑤–78) terminal.)

Turn the DEPTH (PVR3) knob to the left gradually and make sure the voltage at EG terminal is gradually diminished, resulting in  $0 \pm 0.1\text{V}$  when the knob is fully turned to 0 position.

### 3. DE–TUNE Circuit

a. Put the isoration plug into KEYVOLT–IN (J5) on rear panel, connect the KV (④–9, 10) terminal to EK (③–1 ~ 4) terminal with jumper wire and set the MOD VCO2 (PVR4) to 0, then adjust **VR 1** so that  $0 \pm 50\mu\text{V}$  or less is obtained at CP1.

b. Under the condition of item 3–(a), adjust **VR 2** so that  $0 \pm 50\mu\text{V}$  or less is obtainable at CP2.

c. Remove jumper wire and isoration plug next. Let SEQ/KBD switch (PSW4, 5) at KBD, set EG–DEPTH (PVR3) to 0 and turn C<sub>6</sub> key ON after TU (①–1) terminal is set to 0.000V by TURN Volume. (at the time there is 2.000V at KV terminal.)

When CP2 is set at 2.000V by DE–TUNE volume make sure that there is 2.000V at IC6, 7 second pin and also is 166.8mV at IC6, 7 second pin when F<sub>2</sub> key is ON.

### 4. Voltage Control Oscillator Circuit 1 (VCO1) & Wave Shape Convertor Circuit 1 (WSC1)

a. Set both VCO1 and VCO2 SEQ/KBD switches to KBD side, MOD DEPTH (PVR9, 10) are 10, FEET 1 (PSW2) at 2' and turn the TUNE (PVR1) volume untill 0.000V is present at TU (①–1) terminal. Then adjust DE–TUNE (PVR2), when F<sub>2</sub> key is pressed, so that the voltage at CP3 is same as that of CP4 (166.8mV). Next, make sure that voltage of  $2.000 \pm 0.001\text{V}$  is present at CP3 during C<sub>6</sub> key is ON.

b. After the above setting is completed, adjust **VR 4** to achieve  $\square 1$  (④–6) terminal output frequency of 8429Hz when the C<sub>6</sub> key is ON (KV terminal is  $2 \pm 0.001\text{V}$ ).

c. Adjust **VR 3** to achieve 1053.6Hz when the C<sub>3</sub> key is ON (KV terminal is  $250 \pm 0.1\text{mV}$ ).

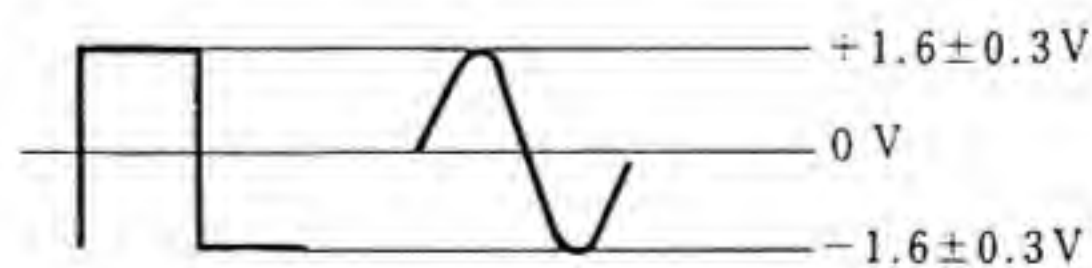
**Note:** Repeat (b) and (c) above so that each frequency variation is within 0.1% even when switching.

d. Check that the frequency is in accordance with the chart below when FEET 1 (PSW2) is switched, as in 4–(b) (i.e., MOD–DEPTH, PWM1, PW1 are 0 and 50%).

| FEET | Frequency (Hz) |
|------|----------------|
| 2'   | 8429           |
| 4'   | 4215           |
| 8'   | 2107           |
| 16'  | 1053.6         |
| 32'  | 526.8          |
| 64'  | 263.4          |

within  $\pm 0.1\%$

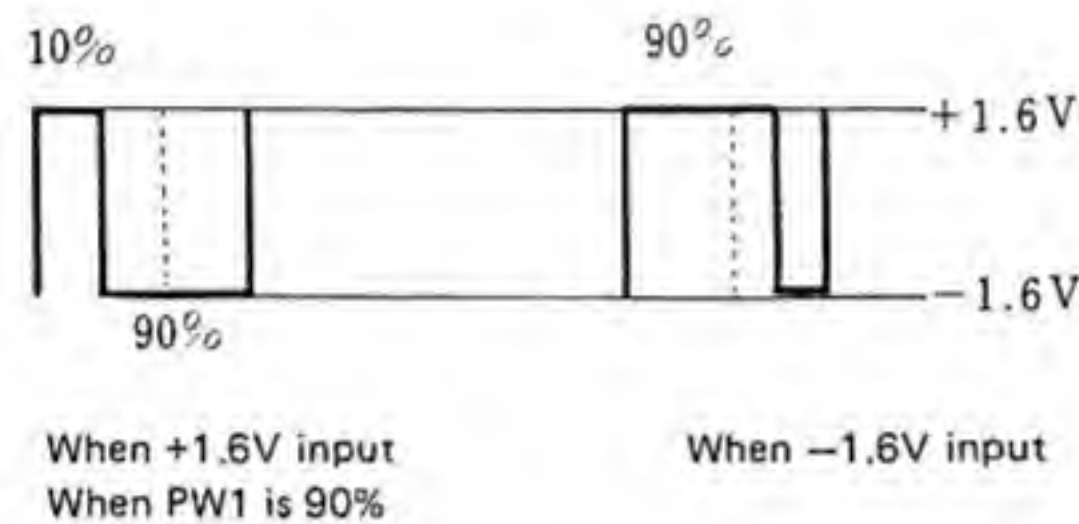
**Note:** The output indicated below should be present at the  $\square 1$  (④–7) and  $\sim 1$  (④–5) terminals when the frequency is the same as the  $\square 1$  terminal.





### 5. PW, PWM Circuit

- Switch the C<sub>6</sub> key ON with FEET 1 (PSW2) at 16', MOD FUNCTION (PSW6) at  $\sim$  and MOD-DEPTH (PVR9) at 10; the frequency should change between 965 and 1150Hz when 3.2Vp-p  $\sim$  wave is added to the  $\sim$  (⑥-1.2) terminal (when the voltage at the  $\sim$  terminal is shifted between +1.6V and -1.6V, the frequency will vary between 965 and 1150Hz). At this time, if the MOD-DEPTH (PVR9) is turned to the left little by little, the frequency variations become less and less; if it is turned all the way to the left, the original frequency ( $1053.6 \pm 1\text{Hz}$ ) should appear.
- Be sure the 3.2Vp-p  $\sim$  wave is added to the  $\sim$  (⑥-1.2) terminal. When PWM1 (PVR7) is at 10, the  $\square$  1 (④-7) terminal receives  $90 \sim 10 \pm 9\%$  duty voltage. Then, when PWM1 (PVR7) is returned to 0, then when PW1 (PVR5) is 90% the  $\square$  1 waveform duty voltage is  $90 \pm 9\%$ .



Note: Inverted wave is fed out from the rear panel OUTPUT.

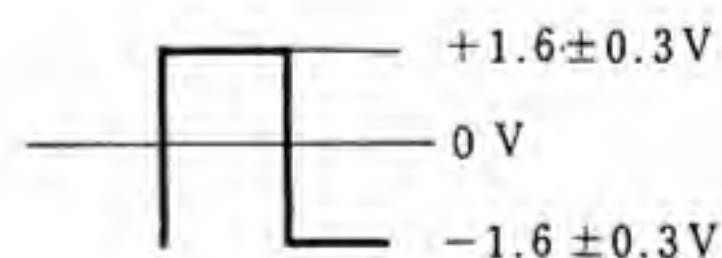
### 6. Voltage Control Oscillator Circuit 2 (VCO2) & Wave Converter Circuit 2 (WSC2)

- As in 4-(a), set FEET 2 (PSW3) to 4'. With the C<sub>6</sub> key ON (KV terminal; 2.000V) adjust VR 8 for 4215Hz at  $\sim$  2 (④-3) terminal.
  - Then, with the C<sub>2</sub> key ON (KV terminal; 250.0mV) adjust VR 7 for 526.8Hz.
- Note: Repeat (a) and (b) above so that each frequency variation is within 0.1% even when switching.
- As in 6-(a), check that the frequency is as indicated in the chart below when FEET 2 (PSW3) is switched.

| FEET | Frequency (Hz) |
|------|----------------|
| 4'   | 4215           |
| 8'   | 2107           |
| 16'  | 1053.6         |
| 32'  | 526.8          |
| 64'  | 263.4          |
| 128' | 131.7          |

within  $\pm 0.1\%$

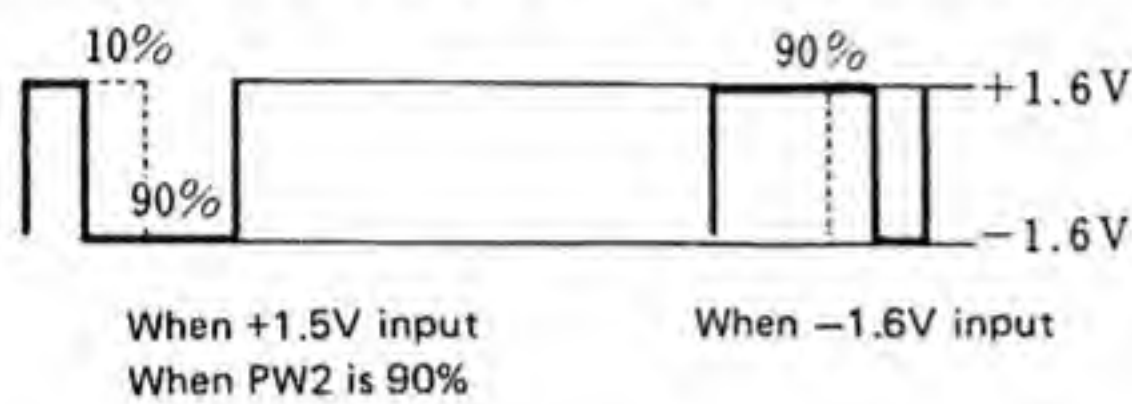
Note: The waveform shown below should be obtained at the  $\square$  2 (④-4) terminal at the same frequencies as  $\sim$  2 terminal.





## 7. PW, PWM Circuit

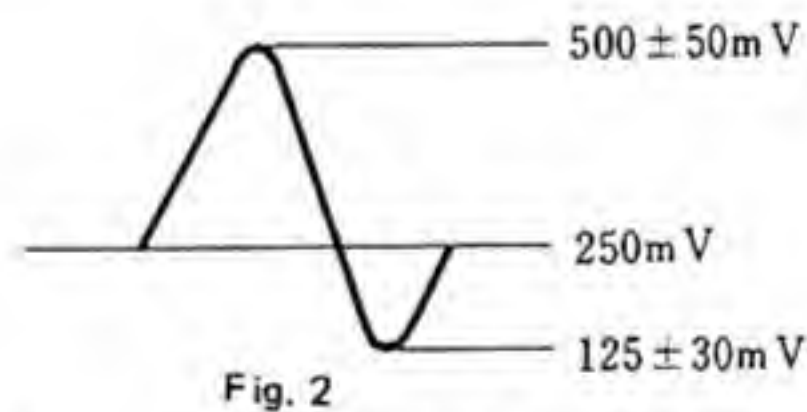
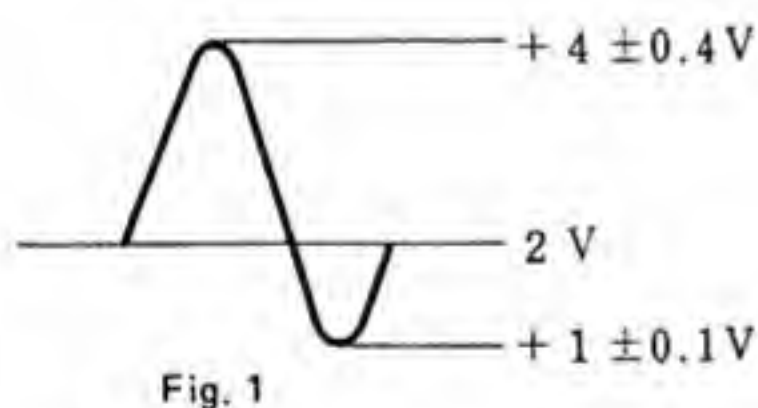
- a. Switch the C<sub>6</sub> key ON, the FEET 2 (PSW3) to 16', MOD FUNCTION (PSW7) to  $\sim$  and MOD-DEPTH (PVR10) to 10. When a 3.2Vp-p  $\sim$  wave is fed to the  $\sim$  (⑥-1.2) terminal the frequency should shift more than 970 ~ 1160Hz (when the voltage at the  $\sim$  terminal is shifted between +1.6V and -1.6V the frequency will vary between 970 and 1160Hz). At this time, if the MOD-DEPTH (PVR10) is turned to the left little by little, the frequency variations become less and less; if it is turned all the way to the left, the original frequency (1053.6Hz) should appear.
- b. Check that a 3.2Vp-p  $\sim$  wave is added to the  $\sim$  (⑥-1.2) terminal. When PWM2 (PVR8) is at 10, the  $\square$  2 terminal (④-4) receives 90 ~ 10  $\pm$  9% duty voltage. Then, when PWM2 is returned to 0 and PW2 (PVR6) is at 90%, the  $\square$  2 waveform duty voltage is 90  $\pm$  9%.



Note: Inverted wave is fed out from the rear panel OUTPUT.

## 8. FM Modulation Circuit

- a. Set the MOD-VCO2 (PVR4) to 10. Then, when the C<sub>6</sub> key is switched ON (KV terminal;  $2 \pm 0.001$  V) adjust **VR 6** at TP1 for a value according to Fig. 1. Now, when the C<sub>3</sub> key is switched ON (KV terminal;  $+250 \pm 0.1$  mV), adjust **VR 5** according to Fig. 2. Repeat these adjustments, making sure there is no deviation in the adjusted value, even during switching.



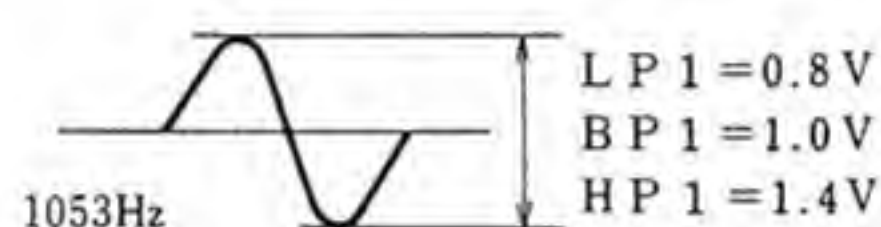
- b. Switch the C<sub>6</sub> key ON (KV terminal,  $+2 \pm 0.001$  V). When MOD-VCO2 (PVR4) is set to 0,  $+2 \pm 0.002$  V should appear at TP1. In this condition, when DE-TUNE (PVR2) is at the [+] side,  $+3 \pm 0.1$  V should appear at TP2; when it is at the [-] side,  $+1.5 \pm 0.1$  V should appear.



## VCF Circuit Board

### 1. Voltage Control Filter Circuit (VCF1)

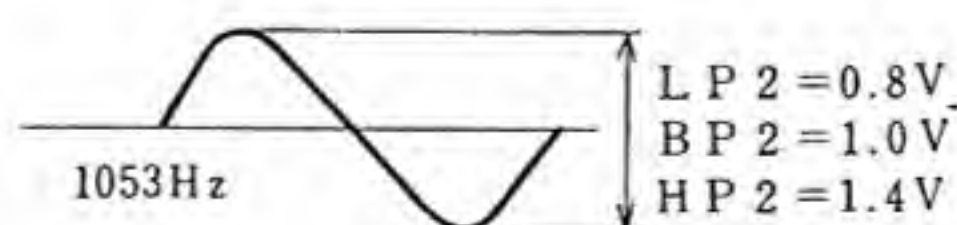
- a. Set INPUT (PSW1) to  $\nearrow$  1 and LEVEL 1 (PVR1) to 10, LEVEL 2 (PVR2), MOD DEPTH (PVR9) and EG-DEPTH (PVR11) to 0 respectively. Then set the VCO1 FEET to 4' and turn the C4 key ON. Add a 3.2Vp-p  $\nearrow$  wave to the  $\nearrow$  1 (①-1) terminal and then adjust CUT OFF FREQ (PVR7) and RESONANCE (PVR5) for +5V at TP2 and TP4.
- b. Under the same conditions as in 1-(a), adjust  $\boxed{\text{VR 1}}$  for peak level and  $\boxed{\text{VR 2}}$  for peak point so that an 0.8Vp-p waveform is present at the LP1 (④-7) terminal.  
Next, the BP1 (④-6) terminal should have a 1.0V output waveform, and HP1 (④-5) terminal should have 1.4V (check that the KV voltage (+500 ± 5mV) is added to the second pin of IC<sub>2</sub>).



- c. Leave adjustments as in 1-(b) and use the CUT OFF FREQ (PVR7) to adjust for a TP2 voltage of +7 ± 0.1V. Then turn the B<sub>5</sub> key ON; when the KBD FOLLOW (PVR3) is set for 500mV at the second pin of IC<sub>1</sub> the LP1 level should just peak.  
Next, when TP2 voltage is +3 ± 0.1V turn the B<sub>2</sub> key ON. When the KBD FOLLOW (PVR3) is used to set for 500mV at the second pin of IC<sub>1</sub> the LP1 level should peak.
- d. Return the settings to the 2-(a, b) condition. When the MOD FUNCTION (PSW4) is set to  $\nearrow$  and MOD DEPTH (PVR9) to 10 check the cutoff frequency by listening to the sound according to the input  $\nearrow$  wave.
- e. Set EG1 ~ 3 to any position and EG DEPTH (PVR11) to approximately center position. Peak frequency should vary according to the EG waveform when the EG SELECTOR (PSW6) is switched from A to E.

### 2. Voltage Control Filter Circuit (VCF2)

- a. Set INPUT (PSW3) to  $\nearrow$  2 and both MOD DEPTH (PVR10) and EG DEPTH (PVR12) to 0. Then set the VCO2 FEET to 4' and turn the C4 key ON. Add a 3.2Vp-p  $\nearrow$  wave to the  $\nearrow$  2 (①-2) terminal and then adjust CUT OFF FREQ (PVR8) and RESONANCE (PVR6) for +5V at TP3 and TP5.
- b. Under the same conditions as in 2-(a), adjust  $\boxed{\text{VR 3}}$  for peak level and  $\boxed{\text{VR 4}}$  for peak point so that an 0.8Vp-p. Waveform is present at the LP2 (④-3) terminal.  
Next, the BP2 (④-2) terminal should have a 1.0V output waveform, and HP2 (④-1) terminal should have 1.4V (check that the KV voltage (+500 ± 5mV) is added to the second pin of IC<sub>2</sub>).





- c. Leave adjustments as in 2—(b) and use the CUT OFF FREQ (PVR8) to adjust for a TP3 voltage of  $+7 \pm 0.1V$ . Then turn the B<sub>5</sub> key ON; when the KBD FOLLOW (PVR4) is set for 500mV at the second pin of IC<sub>2</sub> the LP2 level should just peak.  
Next, when TP3 voltage is  $+3 \pm 0.1V$  turn the B<sub>2</sub> key ON. When the KBD FOLLOW (PVR4) is used to set for 500mV at the second pin of IC<sub>2</sub> the LP2 level should peak.
- d. Return the setting to the 2—(a, b) condition. When the MOD FUNCTION (PSW5) is set to  $\sim$  and MOD DEPTH (PVR10) to 10 check the cutoff frequency by listening to the sound according to the input  $\sim$  wave.
- e. Set EG1 ~ 3 to any position and EG DEPTH (PVR12) to approximately center position. Peak frequency should vary according to the EG waveform when the EG SELECTOR (PSW12) is switched from A to E.


### 3. KBD FOLLOW Circuit

- a. When the F<sub>2</sub> key is ON (with 166.8mV present at the KV (①—7) terminal), adjust VR 7 so that 0mV is present at TP1.
- b. With the KBD FOLLOW (PVR3) set to 0, adjust VR 5 so that the F1I (①—6) terminal receives 166.8mV.  
Then set the KBD FOLLOW (PVR3) to 1 and turn the C<sub>6</sub> key ON. Check for 2.000V at the F1I (①—6) terminal.
- c. As in 3—(a), with the KBD FOLLOW (PVR4) to 0, adjust VR 6 so that 166.8mV appears at the F2I (①—4) terminal.  
Next, set the KBD FOLLOW (PVR4) to 1. Check for 2.000V at the F2I (①—4) terminal when the C<sub>6</sub> key is ON.




## VCA Circuit Board

### 1. Voltage Control Amplifier Circuit No. 1 (VCA1)

- a. Set the VCF1 (PVR1), VCF2 (PVR2),  VCO1 (PVR3) and MOD DEPTH (PVR4) to 0, and set the HOLD/EG switch (PSW5) to HOLD.


Adjust VR 1, when VR 2 is at approximately its center position, so that  $+3 \pm 0.1\text{V}$  is present at TP1.

Then set each of the EG1 ~ 3 sliders to either 0 or S and adjust VR 2 so that  $-200 \pm 10\text{mV}$  is present at TP1 when the HOLD/EG switch (PSW5) is set to EG (i.e., when 0V input is present at the third pin of IC<sub>1</sub>).


After the above adjustments, set the HP/BP/LP switch (PSW2) to HP, the MOD FUNCTION (PSW7) to  and VCF2 (PVR2) to 10.

- b. As in 1—(a), set the HOLD/EG switch (PSW5) to HOLD and the VCO2 FEET to 4'. Adjust the CUT OFF FREQ of VCF2 and the RESONANCE so that a 1053Hz, 3Vp-p waveform is input to the HP2 (①—11) terminal when the C4 key is ON.

At this time adjust VR 3 so that a 1.3Vp-p waveform is present at TP2.

Next set VCF2 (PVR2) to 0, MOD DEPTH (PVR4) to 10 and LFO SPEED to F. Adjust VR 4 so that the TP2 output waveform level is minimum when a 100Hz, 3Vp-p wave is added to the  (②—2) terminal.



### 2. Voltage Control Amplifier Circuit No. 2 (VCA2)

- a. Set the MOD DEPTH (PVR5) to 0, MOD FUNCTION (PSW8) to  and the HOLD/EG switch (PSW6) to HOLD.

When VR 6 is set to approximately its middle position, adjust VR 5 so that  $+3 \pm 0.1\text{V}$  is present at TP3.

Then set each of the EG1 ~ 3 sliders to either 0 or S and adjust VR 6 so that  $-200 \pm 10\text{mV}$  is present at TP3 when the HOLD/EG switch (PSW6) is set to EG (i.e., when 0V input is present at the third pin of IC<sub>3</sub>).

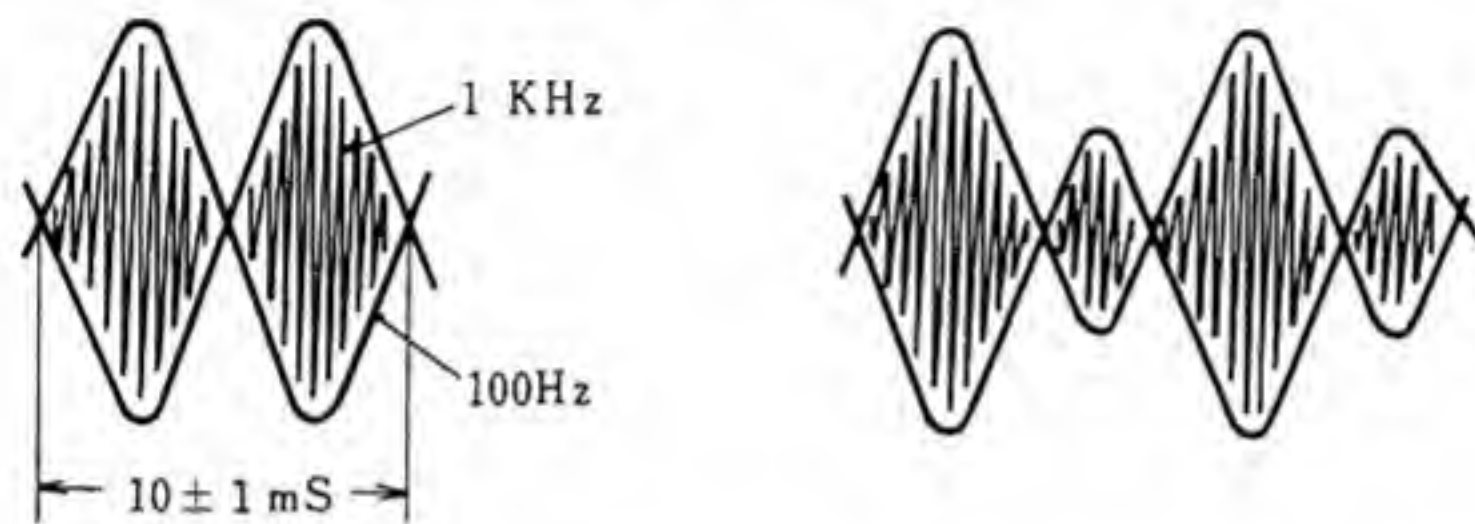
- b. As in 2—(a), set the HOLD/EG switch (PSW6) to HOLD, VCO2 FEET to 4' and switch the C4 key ON. Adjust the VCO2 CUT OFF FREQ and RESONANCE so that a 1053Hz, 3Vp-p waveform is present as input at the HP2 (①—11) terminal. Set the RMO volume (PVR6) to NORMAL. At this time a  $6.6 \pm 0.3\text{V}$  waveform should appear at TP5.

With everything set in this condition, adjust VR 7 so that a  $1.5 \pm 0.05\text{V}$  waveform is present at TP4. Next set the VCO2 section KBD/SEQ switch to SEQ and turn the SEQ section PITCH 1 all the way to the left (so that 0V appears at the HP2 (①—11) terminal). Also set the LFO SPEED to F. Adjust VR 8 so that the TP4 output waveform is minimum when a 100Hz, 3V  waveform is added to the  (②—2) terminal.



### 3. RING MODULATOR Circuit

- a. Set the VCO1/LFO switch (PSW9) to LFO, the RMO volume (PVR6) to MOD and the KBD/SEQ switch in the VCO2 section to SEQ. Then turn the PITCH 1 of the SEQ section all the way to the left (so that 0V appears at the HP2 (①-11) terminal) and set the LFO section SPEED to F. Adjust **VR 9** so that the TP5 signal is minimum when a 100Hz, 3Vp-p  $\sim$  waveform is added to the  $\sim$  (②-2) terminal.
- b. After the above adjustments are made, return the KBD/SEQ switch of the VCO section to KBD and set the VCO2 FEET to 4'. With the C4 key ON (i.e., with a 1KHz, 3V waveform added to the HP2 (①-11) terminal), the waveform shown below should appear at TP5.



If the waveform is unbalanced, take its average.

**Note:** If the waveform is hard to read, adjust the LFO SPEED slightly.



## SEQ Circuit Board

### 1. Clock Pulse Oscillator Circuit

Turn the CLOCK/MANUAL (PSW10) switch to CLOCK and turn the CLOCK SPEED volume (PVR1) to S as far as it will go. Make sure that the frequency is  $0.1 \pm 0.01\text{Hz}$  at TP1. If not, adjust it by turning **VR 2**. Then, turn the CLOCK SPEED volume fully to F position and adjust **VR 1** until  $30 \pm 3\text{Hz}$  is obtained. Repeat this adjustment until both S and F levels are both satisfied. LED indicator must glow in accordance with the frequency.

### 2. Sequencer Circuits

#### A. Step Circuit

- a. After turning the CLOCK/MANUAL (PSW10) switch to CLOCK, STEP (PSW1) selector to 8 and NORMAL/KBD (PSW11) to NORMAL respectively, rotate the CLOCK SPEED volume (PVR1) by about 1/3 of its full extent and depress START/STOP button. The LED indicator should glow to indicate that the steps are shifted from 1 to 8 in sequence.
- b. Turn the STEP (PSW1) switch to [n] position and the step must be changed to 1 to [n] from 1 to 8.

#### B. START/STOP Circuit

After turning the switches as mentioned in paragraph A-(a) above, press START/STOP button ON (+15V input is applied to terminals SP/ST (①-4)). The LED indicator will go off the moment the START/STOP button is depressed and will start from step 1 immediately after the switch is turned ON again.

When CLOCK/MANUAL switch (PSW10) is turned to MANUAL position, the timing step will be halted and it should be shifted step by step turning the START/STOP button ON and OFF alternately.

#### C. Pitch Circuit

After turning the switches as mentioned in paragraph A-(a), rotate each PITCH volume from 1 to 8 (PVR2 to 9) fully in the counterclockwise direction. Adjust **VR 3** so that the voltage level at terminal Q<sub>0</sub> (③-4) is  $0 \pm 50\mu\text{V}$ . Similarly, when all PITCH volumes are turned fully in the clockwise direction,  $2 \pm 0.002\text{V}$  should be obtained at the terminal. With an arbitrary setting of each PITCH volume of 1 to 8, a voltage between 0 and +2V in accordance with the setting should be obtained.

#### D. KV Buffer Circuit

- a. Insert an open plug into KEY VOLT-IN receptacle (J5) on the rear panel and short KV (①-8) across G terminal. When NORMAL/KBD switch (PSW11) is turned to KBD position, the voltage at TP6 must be  $0 \pm 50\mu\text{V}$ . If not, adjust it by means of **VR 4**.
- b. Withdraw the open plug, clear the short circuit and set PITCH 1 (PVR2) volume to the center position. When PITCH volumes 2 to "n" (PVR3 to "n") are fully turned in the clockwise direction,  $+2 \pm 0.002\text{V}$  with the PITCH 1 timing and  $+4 \pm 0.3\text{V}$  with the timing of PITCH 2 to [n] should appear in Q<sub>0</sub> (③-4) terminal.



**E. Hold Circuit**

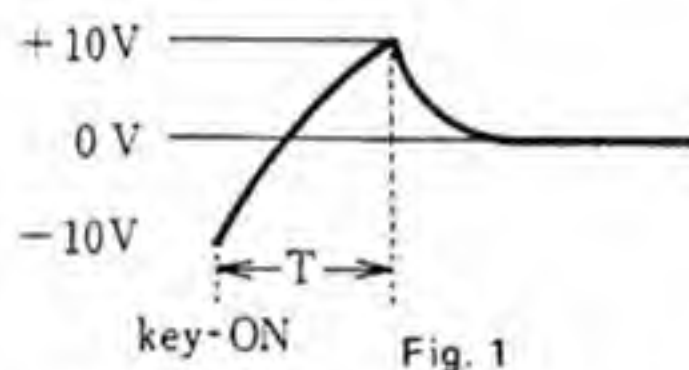
When HOLD button is continuously depressed with the same setting as the above paragraph (a), the voltage levels of  $+2 \pm 0.05\text{V}$  with the timing of PITCH 1 and  $+4 \pm 0.3\text{V}$  with the timing of PITCH 2 to n should appear respectively.

**3. Envelope Generator Circuit****A. EG1**

- a. Respectively turn KBD/SEQ/EXT selector switch (PSW4) to KBD, NORMAL/TIME x 5 switch (PSW7) to NORMAL, INITIAL LEVEL lever (PVR10) to -5, ATTACK LEVEL lever (PVR11) to +5 and DECAY TIME (PVR13) and RELEASE TIME (PVR14) levers to S positions.

Turn the ATTACK TIME Lever (PVR12) until  $+8 \pm 0.1\text{V}$  is obtained at TP3. Adjust **VR 6** so that the rising curve as shown in Fig. 1 with T of  $4 \pm 0.1\text{ms}$  is obtained from terminal A ( $\textcircled{3}-1$ ) when the key is ON ( $-7\text{V}$  is applied to the terminal TR ( $\textcircled{1}-5$ )). In addition, adjust **VR 5** so that the voltage is levelled off at  $0 \pm 0.1\text{V}$  5 seconds or later after the key has been turned ON.

- b. Turn the ATTACK TIME lever until  $+3\text{V} \pm 0.1\text{V}$  is obtained at TP3 and turn the key ON. Adjust **VR 7** to lengthen T when it is longer than  $125\text{ms}$  or to shorten T when it is shorter. Raise the TP3 voltage level to  $+8 \pm 0.1\text{V}$  and adjust **VR 8** again to  $4 \pm 0.1\text{ms}$ . Repeat this adjustment until T becomes  $125 \pm 5\text{ms}$  when  $+3 \pm 0.1\text{V}$  is applied to TP3.



- c. The inverse waveform of terminal A output should be obtained at terminal B ( $\textcircled{3}-3$ ). Confirm that the above T is multiplied by 3.3 to 6.1 when NORMAL/TIME x 5 switch (PSW7) is in TIME x 5 position.

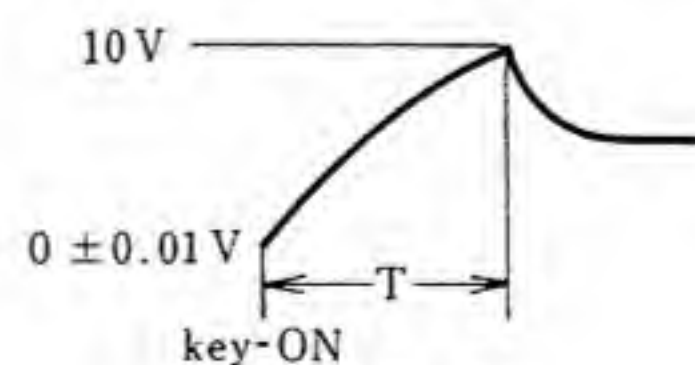
Also make sure that LED indicator (LE9) glows when the key is ON.

**B. EG2**

- a. Respectively turn KBD/SEQ/EXT selector switch (PSW5) KBD, NORMAL/TIME x 5 switch (PSW8) to NORMAL, both DECAY TIME (PVR16) and RELEASE TIME (PVR18) levers to S and SUSTAIN LEVEL lever (PVR17) to 0 positions.

Turn ATTACK TIME lever (PVR15) until  $+8 \pm 0.2\text{V}$  appears at TP4. Adjust **VR 9** so that the rising curve as shown in Fig. 2 is obtained from terminal C ( $\textcircled{3}-7$ ) with T of  $4 \pm 0.1\text{ms}$  when the key is ON ( $-7\text{V}$  is applied to terminal TR ( $\textcircled{1}-5$ )). Also adjust **VR 8** so that the voltage is levelled off at  $0 \pm 0.01\text{V}$  5 seconds or later after the key is ON.

- b. Turn the ATTACK TIME lever until  $+3 \pm 0.1\text{V}$  appears at TP4 and turn the key ON. Adjust **VR10** to lengthen T when it exceeds  $125\text{ms}$  or to shorten T when it is less than that. Raise the voltage level of TP4 to  $+8 \pm 0.1\text{V}$  and adjust **VR 9** again for  $4 \pm 0.1\text{ms}$ . Repeat this adjustment until T becomes  $125 \pm 5\text{ms}$  when TP4 is  $+3 \pm 0.1\text{V}$ .





- c. The inverse waveform of terminal C output should be obtained at terminal D ( 3 —6). Confirm that T above is multiplied by 3.3 to 6.1 when NORMAL/TIME x 5 switch (PSW8) is at TIME x 5 position. Also make sure that LED indicator (LE10) glows when the key is ON.


### C. EG3

- a. Respectively turn KBD/SEQ/EXT selector switch (PSW6) to KBD, NORMAL/TIME x 5 switch (PSW9) to NORMAL, both DECAY TIME (PVR20) and RELEASE TIME (PSW9) levers to S and SUSTAIN LEVEL lever (PVR21) to 0 positions. Turn ATTACK TIME lever (PVR19) until  $+8 \pm 0.2\text{V}$  appears in TP5. Adjust VR12 so that the above rising curve is obtained from terminal E ( 3 —5) with  $4 \pm 0.1\text{mS}$  of T when the key is ON ( $-7\text{V}$  is applied to terminal TR ( 1 —5)). Also adjust VR11 so that the voltage is levelled off at  $0 \pm 0.01\text{V}$  5 seconds or later after the key is turned ON.
- b. Turn ATTACK TIME lever until  $+3 \pm 0.1\text{V}$  appears in TP5. Adjust VR13 to lengthen T when it exceeds  $125\text{mS}$  or to shorten it when it is less than that. Adjust VR12 again so that T becomes  $4 \pm 0.1\text{mS}$  when TP5 is  $+8 \pm 0.1\text{V}$ . Repeat this adjustment until T becomes  $125 \pm 5\text{mS}$  when TP5 is  $+3 \pm 0.1\text{V}$ .
- c. Make sure that T is multiplied by 3.3 to 6.1 when NORMAL/TIME x 5 switch (PSW9) is at TIME x 5 position and that LED indicator (LE11) glows when the key is ON.







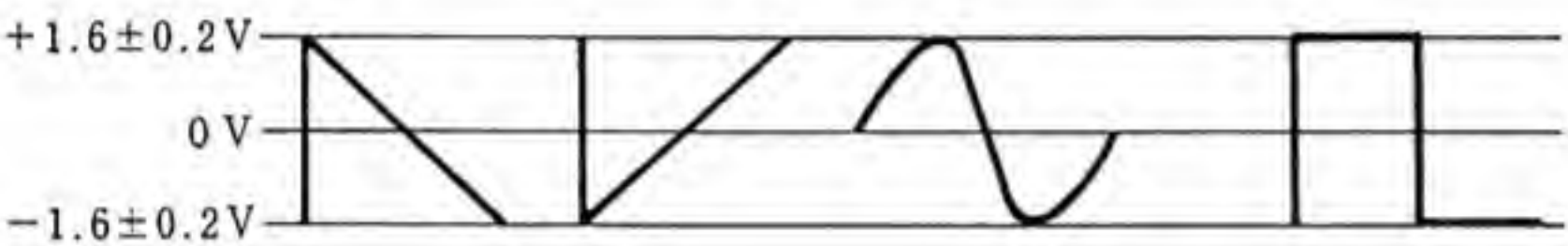
# LFO Circuit Board


## 1. LFO Oscillation Circuit

Turn EG-DEPTH volume (PV1) to 0 and SPEED control (PVR2) to S positions and adjust **VR 2** to provide terminal  (3-8) with  $0.1 \pm 0.02\text{Hz}$ .  
Then, adjust **VR 1** to obtain  $100 \pm 2\text{Hz}$  when SPEED control (PVR2) is turned to F position.  
LED indicator will glow according to the number of frequencies.

## 2. Waveform Conversion Circuit

a. The waveforms shown in Fig. 1, Fig. 2, Fig. 3 and Fig. 4 should be obtained at terminals  (3-8),  (3-7),  (3-9) and  (4-1) respectively.



b. When LFO/NORMAL switch on TRIGGER is turned to LFO (0V at terminal N (4-2) and the key is turned ON (-7V is applied to terminal KTR (4-3)), the waveform shown in Fig. 5 should be obtained at terminal O  (3-10) and its frequency should be one half (cycle time is two times that of LFO oscillator.)

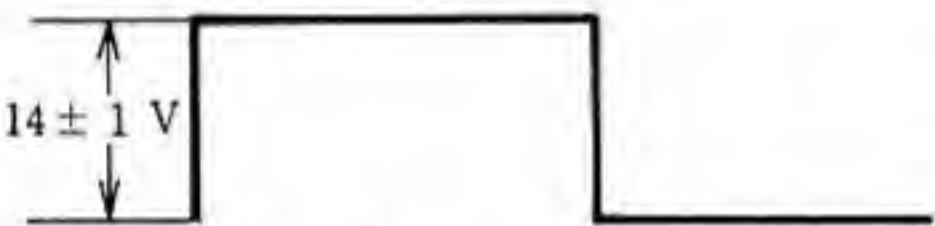


Fig. 5

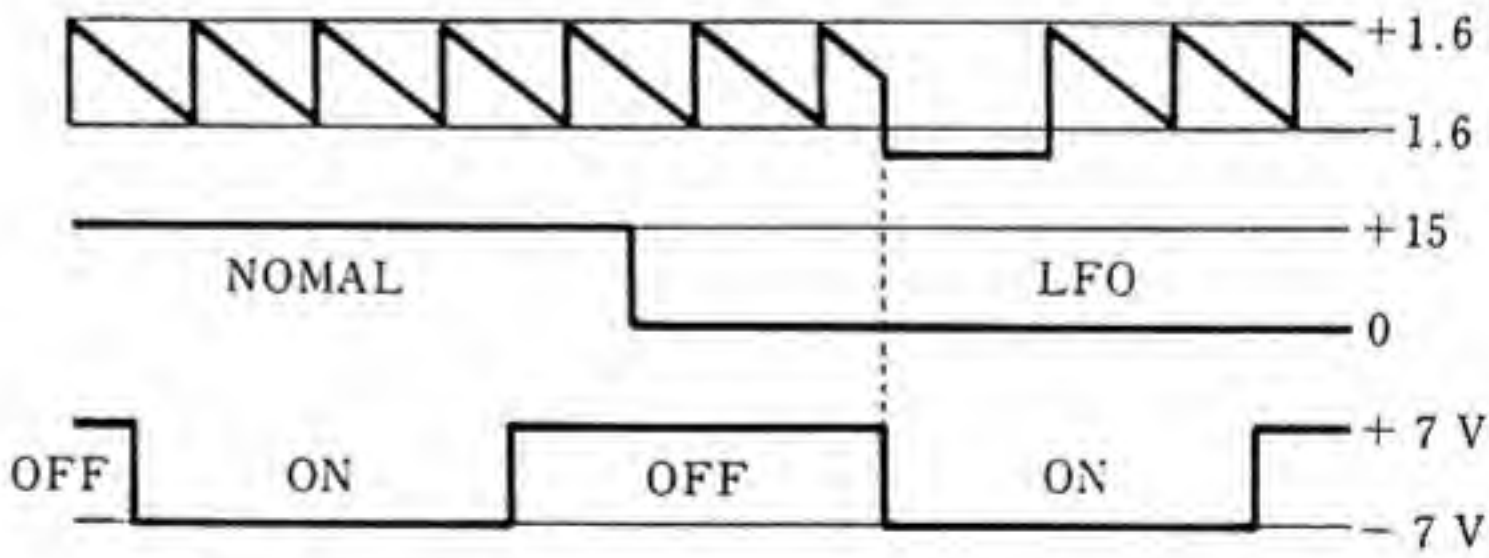
## 3. Trigger Circuit

Terminal LTR (4-7) should operate as shown in Fig. 4 under the following conditions:

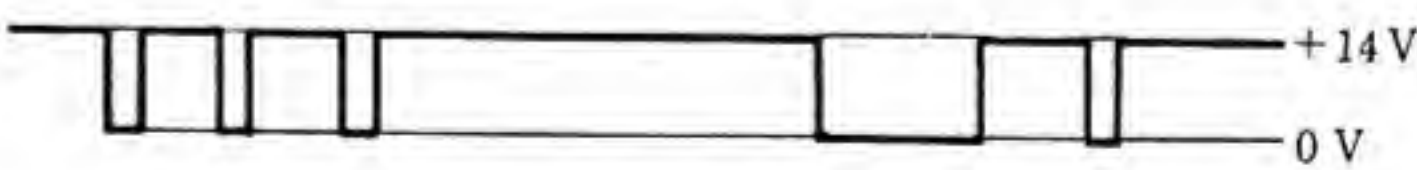
LFO oscillation terminal (3-8)

LFO/NOR . . . . . N terminal (4-2)

KEY-ON . . . . . KTR terminal (4-3)



LTR terminal (4-7)



LED glows



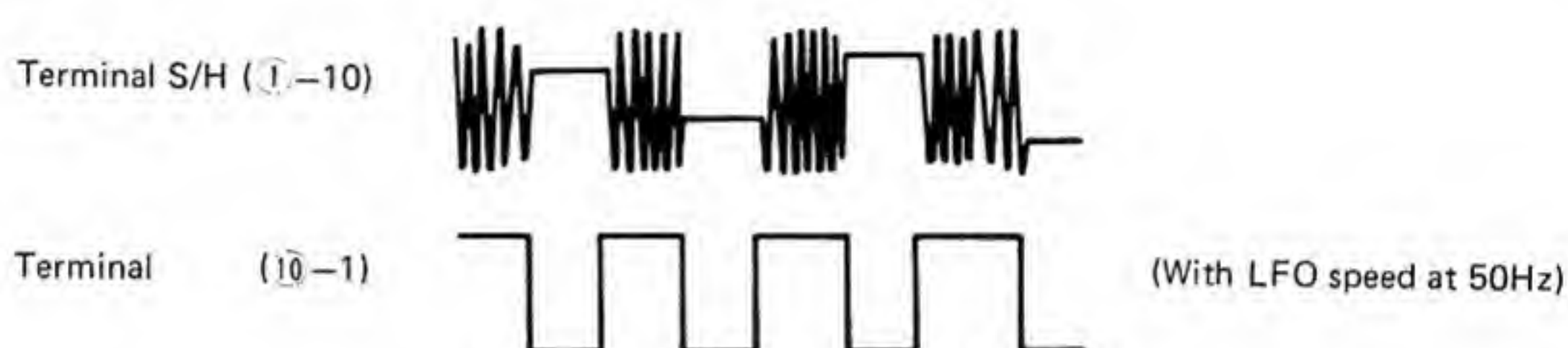


#### 4. Noise Generator Circuit

- a. Adjust **VR 3** to obtain  $5 \pm 1$  Vp-p (2 dBm) output at terminal NI (2-1).



- b. Adjust **VR 4** so that voltage fluctuates at terminal S/H (1-10) to an equal degree above and below 0V as the center, as illustrated below:



#### 5. EXT Pre-amplifier Circuit

- a. Set FEET on VCO1 to 8',  $\wedge$  VCO1 on VCA1 to 10, and all others to 0, and turn EG/HOLD selector switch to HOLD.  
Then, set BALANCE on PN3 to 1 and adjust VOLUME to provide OUTPUT 1 with a 20mV (−40 dBm) output level when key C4 is turned ON (1053Hz output).  
Now, connect OUTPUT 1 to EXTERNAL-IN by using a guitar lead (20mV, 1053Hz is applied to terminal ESI (2-7)).
- b. After the completion of the setting mentioned in paragraph 5-a, 120mV output should be obtained at terminal 0 (2-5) when SIGNAL LEVEL (PVR4) is turned to 10. Also, 1.25V output should be presented at terminal −20 (2-3).

#### 6. EXT Trigger Circuit

In addition to the same setting as mentioned in paragraph 5-(a), set TRIGGER LEVEL (PVR3) to 10 and −20/0 selector switch on the rear panel to the 0 position. When SIGNAL LEVEL is set so that a voltage of  $+60 \pm 5$  mV is applied at terminal ETI (4-6),  $0 \pm 0.2$  V output should appear at terminal ETO (4-5).

In addition, when SIGNAL LEVEL is set to 0, +15V output should be obtained at terminal ETO.



## PRA Circuit Board

### 1. Amplifier Circuit

Set the PN3 VOLUME to MAX and make sure that an input signal of about 0.3V is applied to terminals 1I (①-7) and 2I (①-9) respectively when the key is turned ON. Then, adjust **VR1** and **VR2** so that 0.6V signal appears at terminals 1H (①-5) and 2H (①-13) respectively.

At this stage, 100mV output must be obtained from terminals 1L (①-2) and 2L (①-11) respectively, and also 0.6V output from 1 + 2H (②-2) and 50mV output from 1 + 2L (①-15) terminals.

### 2. Headphone Amplifier Circuit

When a set of headphones (8 ohm) is connected to the PHONES jack on PN3, 250mV output should be obtained from terminals HR (②-13) and HL (②-12).

### 3. Initial Clear Circuit

Connect either a set of headphones or a guitar amplifier, turn the key ON and make sure that a sound is produced. Turn the main switch OFF and then turn it ON after 10 seconds. A sound should be heard about 8 seconds after the main switch has been turned ON.

### 4. Foot Controller Current Regulation Circuit

A  $+14 \pm 1V$  and  $-14 \pm 1V$  should be obtained from terminals +X (②-15) and -X (②-14) respectively.



# **YAMAHA**      **COMBO SYNTHESIZER**

## **CS-30**

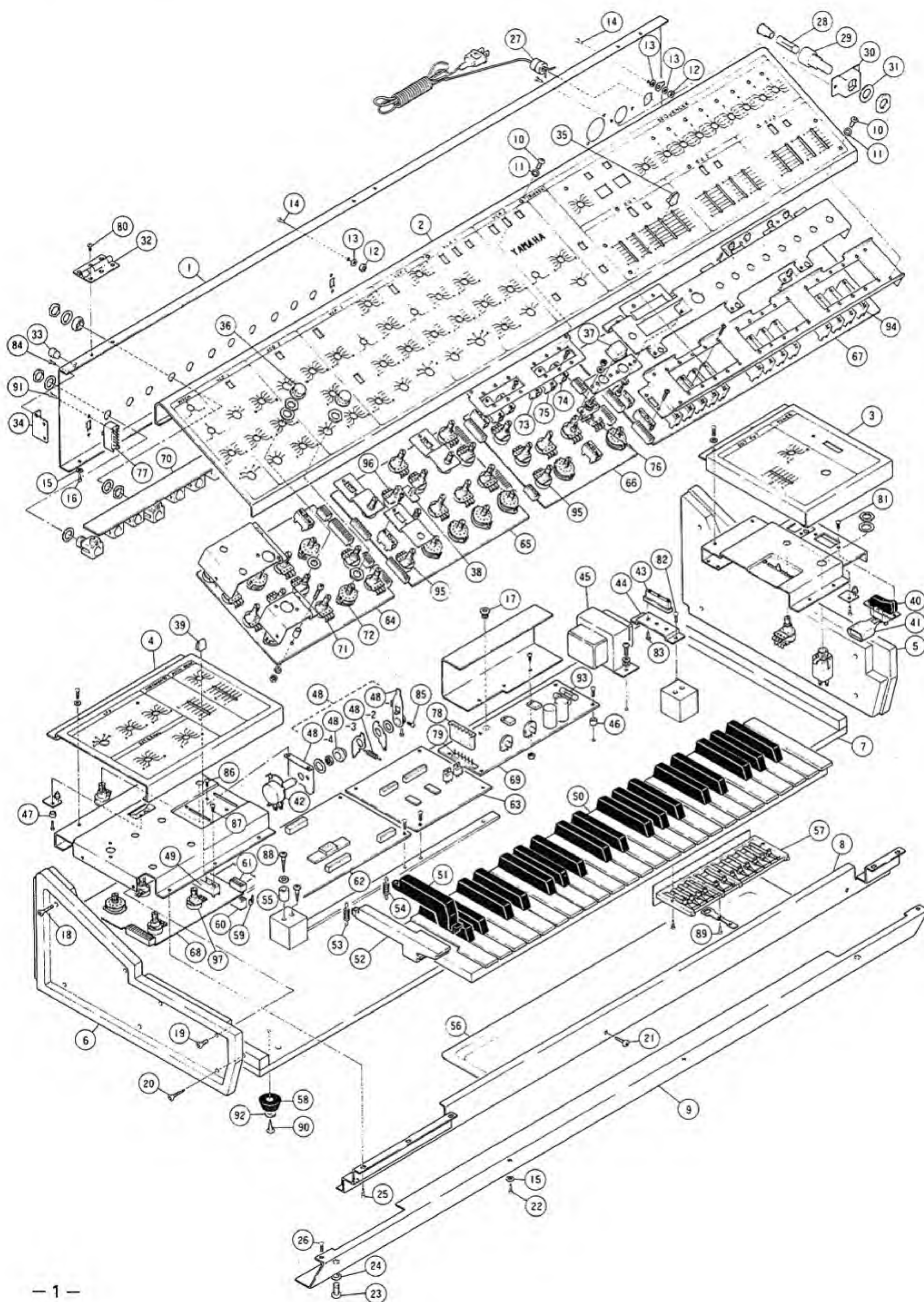
### **PARTS LIST**



#### INDEX (目次)

|                                                |   |
|------------------------------------------------|---|
| Circuit Boards & Components (シート及びシート部品) ..... | 2 |
| Keyboard, Panel & Components (鍵盤及びパネル部品) ..... | 5 |
| Cabinet (外装部品) .....                           | 7 |







## 1. Circuit Boards &amp; Components(シート及びシート部品)

| Ref. No. | Part No.             | Description (部 品 名)           | Remarks      | Common Model           |           |  |
|----------|----------------------|-------------------------------|--------------|------------------------|-----------|--|
| 62       | 30:12:47:NA:80:28:80 | SSK circuit board #82580      | S S K シ ー ト  | CS-30L                 |           |  |
| 64       | 30:12:47:NA:80:28:90 | VCO -- do. -- #82590          | V C O シ ー ト  |                        |           |  |
| 65       | 30:12:47:NA:80:29:00 | VCF -- do. -- #82600          | V C F シ ー ト  |                        |           |  |
| 66       | 30:12:47:NA:80:29:10 | VCA -- do. -- #82610          | V C A シ ー ト  |                        |           |  |
| 63       | 30:12:47:NA:80:29:20 | PRA -- do. -- #82620          | P R A シ ー ト  | CS-30L                 |           |  |
| 67       | 30:12:47:NA:80:29:30 | SEQ -- do. -- #82630          | S E Q シ ー ト  |                        |           |  |
| 68       | 30:12:47:NA:80:29:40 | LFO -- do. -- #82641          | L F O シ ー ト  |                        |           |  |
| 70       | 30:12:00:NA:80:29:50 | JK -- do. -- #82650           | J K シ ー ト    |                        |           |  |
| 69       | 30:12:00:NA:80:29:60 | ADC -- do. -- #82640          | A D C シ ー ト  | CS-30L                 |           |  |
|          | 30:12:00:NA:80:29:70 | -- do. -- -- do. -- -- do. -- | "            | N. European British    | -- do. -- |  |
|          | 30:12:00:NA:80:36:40 | -- do. -- -- do. -- -- do. -- | "            | Japan                  | -- do. -- |  |
|          |                      |                               |              |                        |           |  |
|          | 30:10:00:YM:24:80:00 | IC YM24800                    | I C          | SSK                    |           |  |
|          | 40:10:00:IG:00:10:20 | -- do. -- HA1452              | "            | OP-Amp                 |           |  |
|          | 40:10:00:IG:00:12:40 | -- do. -- TC4011              | "            | NAND                   |           |  |
|          | 40:10:00:IG:00:12:60 | -- do. -- TC4049              | "            | Inverter               |           |  |
|          | 40:10:00:IG:00:13:90 | -- do. -- NJM4558             | "            | OP-Amp                 |           |  |
|          | 40:10:00:IG:00:15:00 | -- do. -- IG00150             | "            | VCOII                  |           |  |
|          | 40:10:00:IG:00:15:10 | -- do. -- IG00151             | "            | VCA                    |           |  |
|          | 40:10:00:IG:00:15:20 | -- do. -- IG00152             | "            | EG-VCF                 |           |  |
|          | 40:10:00:IG:00:15:30 | -- do. -- IG00153             | "            | VCOIII                 |           |  |
|          | 40:10:00:IG:00:15:60 | -- do. -- IG00156             | "            | VCF                    |           |  |
|          | 40:10:00:IG:00:15:80 | -- do. -- IG00158             | "            | WSC                    |           |  |
|          | 40:10:00:IG:00:15:90 | -- do. -- IG00159             | "            | EG-VCA                 |           |  |
|          | 40:10:00:IG:00:16:00 | -- do. -- BA634               | "            | Divider                |           |  |
|          | 40:10:00:IG:00:16:20 | -- do. -- $\mu$ A796HC        | "            | Ring-MOD               |           |  |
|          | 40:10:00:IG:00:16:90 | -- do. -- TC4016P             | "            | Gate                   |           |  |
|          | 40:10:00:IG:00:17:20 | -- do. -- TC4069P             | "            | Inverter               |           |  |
|          | 40:10:00:IG:02:55:00 | -- do. -- TA7504S             | "            | OP-Amp                 |           |  |
|          | 40:10:00:IG:02:56:00 | -- do. -- TA7505              | "            | OP-Amp                 |           |  |
|          | 40:10:00:IG:02:75:00 | -- do. -- TC4022P             | "            | 8 step counter         |           |  |
|          |                      |                               |              |                        |           |  |
|          | 40:10:00:IA:04:90:10 | Transistor 2SA490             | ト ラ ン ジ ス タ  |                        |           |  |
|          | 40:10:00:IA:05:61:70 | -- do. -- 2SA561              | "            |                        |           |  |
|          | 40:10:00:IC:04:58:50 | -- do. -- 2SC458              | "            |                        |           |  |
|          | 40:10:00:IC:05:09:20 | -- do. -- 2SC509              | "            |                        |           |  |
|          | 40:10:00>ID:02:35:10 | -- do. -- 2SD235              | "            |                        |           |  |
|          |                      |                               |              |                        |           |  |
|          | 40:10:00:IE:00:00:10 | FET 2SK30A                    | F E T        |                        |           |  |
|          |                      |                               |              |                        |           |  |
|          | 40:10:00:IF:00:00:10 | Diode 1N34A                   | ダ イ オ ー ド    |                        |           |  |
|          | 40:10:00:IF:00:00:40 | -- do. -- 1S1555              | "            |                        |           |  |
|          | 40:10:00:IF:00:03:00 | -- do. -- 1S1715P             | "            |                        |           |  |
|          | 40:10:00:iH:00:01:40 | -- do. -- 10DC-4              | "            | Substitution of 10DC-1 |           |  |
|          | 40:10:00:iH:00:01:50 | -- do. -- 10DC-4R             | "            | -- do. -- of 10DC-1R   |           |  |
|          | 40:10:00:iH:00:05:90 | -- do. -- 10E-1               | "            |                        |           |  |
|          |                      |                               |              |                        |           |  |
|          | 40:10:00:IF:00:04:20 | Zener Diode 02Z5.6A           | ツェナーダイオード    |                        |           |  |
|          | 40:10:00:IF:00:07:80 | -- do. -- WZ150               | "            |                        |           |  |
|          | 40:10:00:IF:00:09:90 | -- do. -- 02Z7.5A             | "            |                        |           |  |
|          |                      |                               |              |                        |           |  |
|          | 40:10:00:IF:00:06:80 | Light Emitted Diode SLP132B   | 発 光 ダイ オ ー ド |                        |           |  |



| Ref. No. | Part No.             | Description (部 品 名)                        | Remarks         | Common Model |  |  |
|----------|----------------------|--------------------------------------------|-----------------|--------------|--|--|
|          | 40:10:00:IK:00:01:10 | Photo Coupler P588-G50-201B                | フ ォ ト カ ブ ラ ー   |              |  |  |
|          | 40:10:00:FF:04:31:20 | Polystyrene Capacitor 1,200PF              | スチロールコンデンサ      |              |  |  |
|          | 40:10:00:FC:08:54:70 | Mylar Capacitor 100V 0.47 $\mu$ F          | マイラーコンデンサ       |              |  |  |
|          | 40:10:00:FM:09:71:00 | Nonpolar Capacitor 16V 10 $\mu$ F          | N P コ ン デ ン サ   |              |  |  |
|          | 40:10:00:FP:14:61:00 | Tantalum Capacitor 25V 1 $\mu$ F           | タンタルコンデンサ       |              |  |  |
|          | 40:10:00:FP:15:53:30 | - do. - 35V 0.33 $\mu$ F                   | "               |              |  |  |
|          | 40:10:00:FP:15:56:80 | - do. - - do. - 0.68 $\mu$ F               | "               |              |  |  |
|          | 40:10:00:Hu:19:51:00 | Metal Film Resistor 0.1% 100 $\Omega$      | 金 属 被 膜 抵 抗     |              |  |  |
|          | 40:10:00:Hu:19:61:00 | - do. - - do. - 1 K $\Omega$               | "               |              |  |  |
|          | 40:10:00:Hu:19:62:00 | - do. - - do. - 2 K $\Omega$               | "               |              |  |  |
|          | 40:10:00:Hu:19:65:00 | - do. - - do. - 5 K $\Omega$               | "               |              |  |  |
|          | 40:10:00:Hu:19:71:00 | - do. - - do. - 10 K $\Omega$              | "               |              |  |  |
|          | 40:10:00:Hu:19:72:00 | - do. - - do. - 20 K $\Omega$              | "               |              |  |  |
|          | 40:10:00:Hu:19:74:00 | - do. - - do. - 40 K $\Omega$              | "               |              |  |  |
|          | 40:10:00:Hu:19:78:00 | - do. - - do. - 80 K $\Omega$              | "               |              |  |  |
|          | 40:10:00:Hu:19:81:00 | - do. - - do. - 100 K $\Omega$             | "               |              |  |  |
|          | 40:10:00:Hu:19:81:60 | - do. - - do. - 160 K $\Omega$             | "               |              |  |  |
|          | 40:10:00:HZ:00:08:60 | - do. - - do. - 29.94 K $\Omega$           | "               |              |  |  |
|          | 40:10:00:HZ:00:08:80 | - do. - - do. - 1.684 K $\Omega$           | "               |              |  |  |
|          | 40:10:00:Hu:57:53:30 | - do. - 1% 330 $\Omega$                    | "               |              |  |  |
|          | 40:10:00:Hu:57:59:10 | - do. - - do. - 910 $\Omega$               | "               |              |  |  |
|          | 40:10:00:Hu:57:61:00 | - do. - - do. - 1 K $\Omega$               | "               |              |  |  |
|          | 40:10:00:Hu:57:62:00 | - do. - - do. - 2 K $\Omega$               | "               |              |  |  |
|          | 40:10:00:Hu:57:65:10 | - do. - - do. - 5.1 K $\Omega$             | "               |              |  |  |
|          | 40:10:00:Hu:57:68:20 | - do. - - do. - 8.2 K $\Omega$             | "               |              |  |  |
|          | 40:10:00:Hu:57:71:00 | - do. - - do. - 10 K $\Omega$              | "               |              |  |  |
|          | 40:10:00:Hu:57:71:80 | - do. - - do. - 18 K $\Omega$              | "               |              |  |  |
|          | 40:10:00:Hu:57:72:20 | - do. - - do. - 22 K $\Omega$              | "               |              |  |  |
|          | 40:10:00:Hu:57:81:00 | - do. - - do. - 100 K $\Omega$             | "               |              |  |  |
|          | 40:10:00:HL:31:24:70 | Metal oxide Film Resistor 1W 0.47 $\Omega$ | 酸 化 金 属 被 膜 抵 抗 |              |  |  |
|          | 40:10:00:HL:32:34:70 | - do. - 2W 4.7 $\Omega$                    | "               |              |  |  |
|          | 40:10:00:HL:32:41:00 | - do. - 2W 10 $\Omega$                     | "               |              |  |  |
|          | 40:10:00:Hi:20:99:90 | Solid Resistor 10M $\Omega$                | ソ リ ッ ド 抵 抗     |              |  |  |
|          | 40:10:00:HT:37:01:50 | Semi Variable Resistor B-100 $\Omega$      | 半 固 定 抵 抗       | V8K-4-1 type |  |  |
|          | 40:10:00:HT:37:01:60 | - do. - B-200 $\Omega$                     | "               | - do. -      |  |  |
|          | 40:10:00:HT:37:00:10 | - do. - B-1K $\Omega$                      | "               | - do. -      |  |  |
|          | 40:10:00:HT:37:00:20 | - do. - B-10K $\Omega$                     | "               | - do. -      |  |  |
|          | 40:10:00:HT:37:01:00 | - do. - B-50K $\Omega$                     | "               | - do. -      |  |  |
|          | 40:10:00:HT:37:00:30 | - do. - B-100K $\Omega$                    | "               | - do. -      |  |  |
|          | 40:10:00:HT:37:01:10 | - do. - B-200K $\Omega$                    | "               | - do. -      |  |  |
|          | 40:10:00:HT:37:01:30 | - do. - B-500K $\Omega$                    | "               | - do. -      |  |  |
|          | 40:10:00:HT:37:01:40 | - do. - B-1M $\Omega$                      | "               | - do. -      |  |  |
|          | 40:10:00:HT:14:01:70 | - do. - B-2 K $\Omega$                     | "               | V18K type    |  |  |
|          | 40:10:00:HT:55:00:60 | - do. - B-5 K $\Omega$                     | "               | 3006P type   |  |  |







CS-30(S/# 1001~)

## 2. Keyboard, Panel & Components(鍵盤及びパネル部品)

| Ref. No. | Part No.             | Description (部 品 名)                          | Remarks    | Common Model                              |  |  |
|----------|----------------------|----------------------------------------------|------------|-------------------------------------------|--|--|
| 50       | 30 12 47 NB 80 78 90 | Keyboard Assembly                            | 鍵盤 Ass'y   |                                           |  |  |
| 57       | 30 12 47 NB 80 78 80 | Switch Assembly 1U                           | スイッチ Ass'y |                                           |  |  |
|          | 30 12 46 NB 80 77 90 | - do. - 2, 3, 4U                             | "          |                                           |  |  |
| 52       | 30 10 00 CB 01 11 70 | White Key C, F                               | 白 鍵        |                                           |  |  |
|          | 30 10 00 CB 01 11 80 | - do. - D                                    | "          |                                           |  |  |
|          | 30 10 00 CB 01 11 90 | - do. - B, E                                 | "          |                                           |  |  |
|          | 30 10 00 CB 01 12 00 | - do. - G                                    | "          |                                           |  |  |
|          | 30 10 00 CB 01 12 10 | - do. - A                                    | "          |                                           |  |  |
|          | 30 10 00 CB 01 12 20 | - do. - C'                                   | "          |                                           |  |  |
| 51       | 30 10 00 CB 01 12 30 | Black Key                                    | 黒 鍵        |                                           |  |  |
| 53       | 30 10 00 AA 01 56 70 | Key Spring for White Key                     | キースプリング    |                                           |  |  |
| 54       | 30 10 00 AA 01 56 80 | - do. - for Black Key                        | "          |                                           |  |  |
| 35       | 30 10 00 CB 81 12 90 | Knob for Slide VR                            | つまみ        |                                           |  |  |
| 36       | 30 10 00 CB 81 01 30 | - do. - for Rotary VR                        | "          |                                           |  |  |
| 37       | 30 10 00 CB 81 03 90 | - do. - for Push SW                          | "          |                                           |  |  |
| 38       | 30 54 00 CB 80 52 30 | - do. - for Slide SW                         | "          |                                           |  |  |
| 39       | 30 10 00 CB 81 12 80 | - do. - for Slide VR                         | "          | PITCH BEND<br>PORTAMENTO                  |  |  |
| 77       | 40 10 00 KA 40 02 50 | Slide Switch                                 | スライド S W   | -20/0<br>OUTPUT High/Low                  |  |  |
|          | 40 10 00 HS 31 02 40 | Variable Resistor A-50 K $\Omega$ $\times$ 2 | 可変抵抗器      | VOLUME                                    |  |  |
|          | 40 10 00 HS 31 03 00 | - do. - C-50 K $\Omega$                      | "          | LIMITTER                                  |  |  |
| 42       | 40 10 00 HS 42 02 70 | - do. - W-50 K $\Omega$                      | "          | PITCH BEND                                |  |  |
| 49       | 40 10 00 HQ 42 00 40 | Slide Variable Resistor A-2M $\Omega$        | スライド V R   | PORTAMENTO                                |  |  |
|          | 40 10 00 HQ 42 00 50 | - do. - MN-10 K $\Omega$                     |            | BALANCE                                   |  |  |
| 28       | 40 10 00 KB 00 06 60 | Fuse 250V 400 mAT                            | ヒューズ       | N.European<br>British                     |  |  |
|          | 40 10 00 KB 00 11 50 | - do. - 0.5 AT                               | "          | Australian                                |  |  |
|          | 40 10 00 KB 00 10 60 | - do. - 1 A                                  | "          | others                                    |  |  |
|          | 40 10 00 KB 00 02 10 | - do. - 125V 1 AT                            | "          | Japan                                     |  |  |
| 29       | 40 10 00 LB 20 04 90 | Fuse Holder                                  | ヒューズホルダー   |                                           |  |  |
|          | 40 10 00 LB 20 05 90 | - do. -                                      | "          | British, North European                   |  |  |
|          | 40 10 00 LB 20 02 50 | Voltage Selector                             | 電圧切替器      | General, S.African<br>British, N.European |  |  |
| 45       | 40 10 00 GA 80 56 00 | Power Transformer                            | 電源トランス     | Japan, US.American,<br>Canadian           |  |  |
|          | 30 12 00 NB 80 80 50 | Power Transformer Unit with Connector        | 電源トランスユニット | others                                    |  |  |
| 40       | 40 10 00 KA 10 05 50 | Power Switch                                 | パワースイッチ    | Japan, US.American<br>Canadian            |  |  |
|          | 40 10 00 KA 10 05 60 | - do. -                                      | "          | others                                    |  |  |
| 41       | 40 10 00 FZ 00 09 50 | Spark Suppressor Capacitor 250V 0.033 + 120  | スパークキラー    | Canadian                                  |  |  |
|          | 40 10 00 FZ 00 01 10 | - do. - 125V 0.033 + 120                     | "          | Japan, US.American                        |  |  |
|          | 40 10 00 FQ 02 44 70 | - do. - oil capacitor 630V 0.047 $\mu$       | "          | GENERAL, S.African                        |  |  |
| 27       | 40 10 00 CB 07 27 50 | Bush for Cord                                | コードブッシュ    | Japan                                     |  |  |
|          | 40 10 00 CB 81 12 30 | - do. -                                      | "          | US.American Canadian                      |  |  |
|          | 40 10 00 CB 07 06 90 | - do. -                                      | "          | others                                    |  |  |



[illegible]



### 3. Cabinet (外装部品)

[illegible]